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# EDN®

Designer's guide to dynamic RAMs—Part 2

Graphing software plots sophisticated numerical data

Use dual-port static RAMs for tricky interface problems

NuBus interface options



ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

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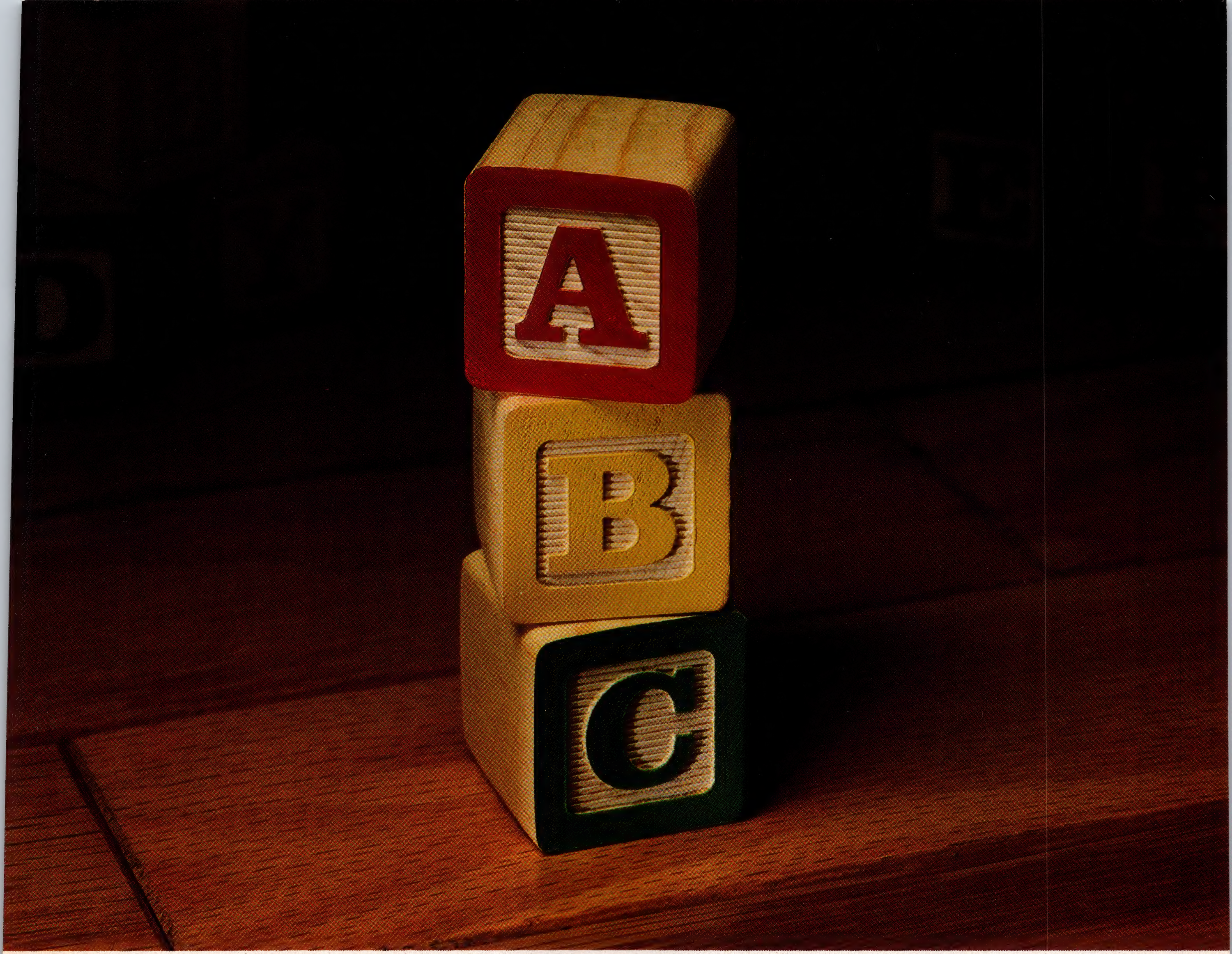


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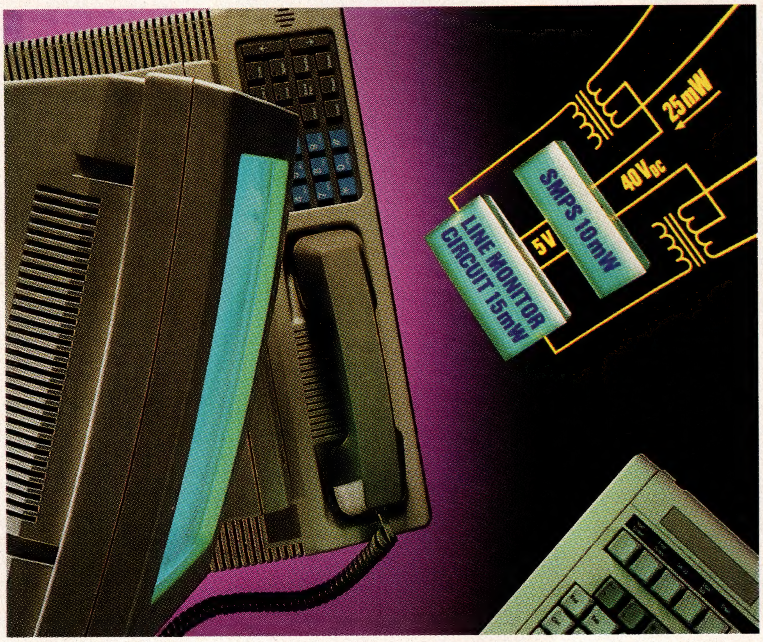


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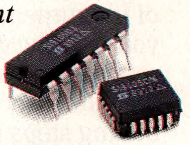

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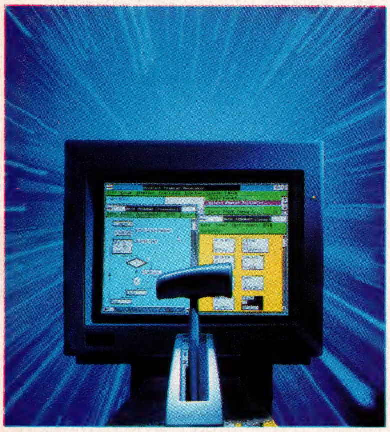
EDN Magazine Edition

Volume 34, Number 8

April 13, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



***On the cover:*** *IEEE software packages featuring instrument function panels let you use simple English commands to set or change instrument controls. The software then automatically generates IEEE-488 control programs. See pg 142. (Photo courtesy Wavetek Corp)*

## SPECIAL REPORT



## DESIGN FEATURES



*Continued on page 7*

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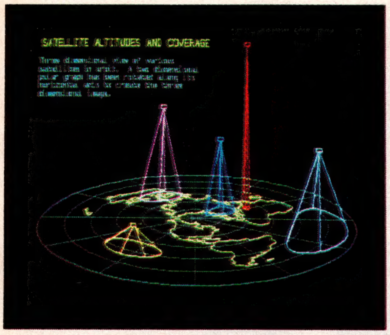
*Continued from page 5*






***Graphing software packages** enable today's small computers to plot almost any numerical information (pg 53).*

EDN magazine now offers Express Request, a convenient way to retrieve product information by phone. See the Reader Service Card in the front for details on how to use this free service.

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## TECHNOLOGY UPDATE



## PRODUCT UPDATE



## DESIGN IDEAS



*Continued on page 9*

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A look at the video-game market shows what can happen when a manufacturer uses electronics to stifle a market instead of letting it expand.

## NEW PRODUCTS



## PROFESSIONAL ISSUES 283

Improving working conditions for engineers: Should the IEEE do more?—*Paul Kinnucan*

## LOOKING AHEAD 299

Consumers are unaware of fax for personal computers . . . NASA information-systems budget to increase to $1.3B.

## DEPARTMENTS


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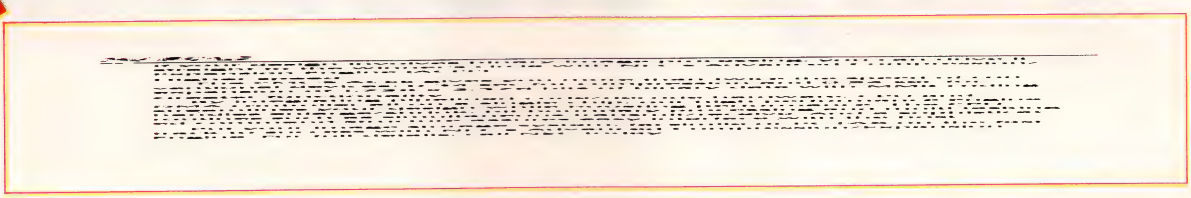

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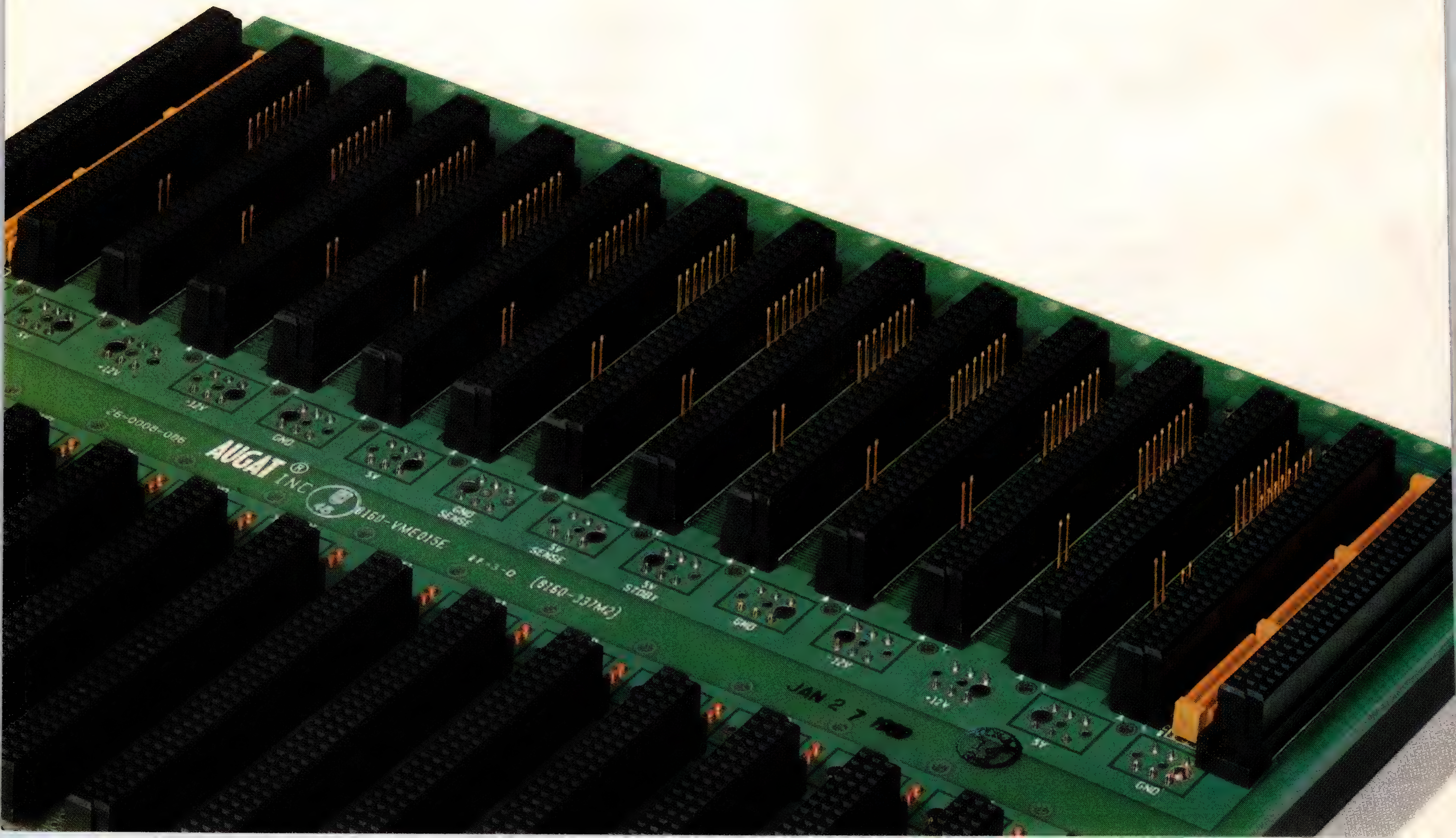

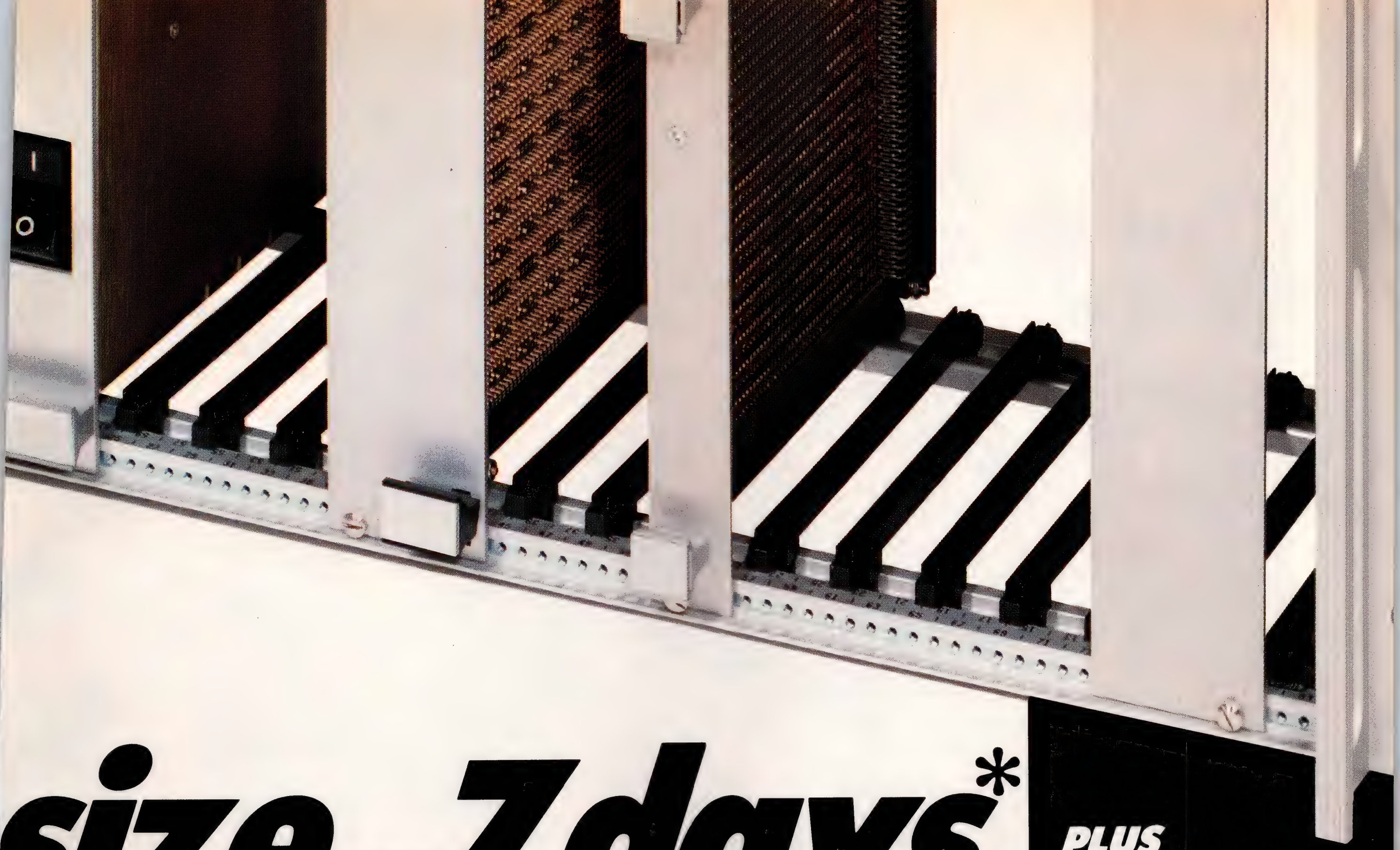

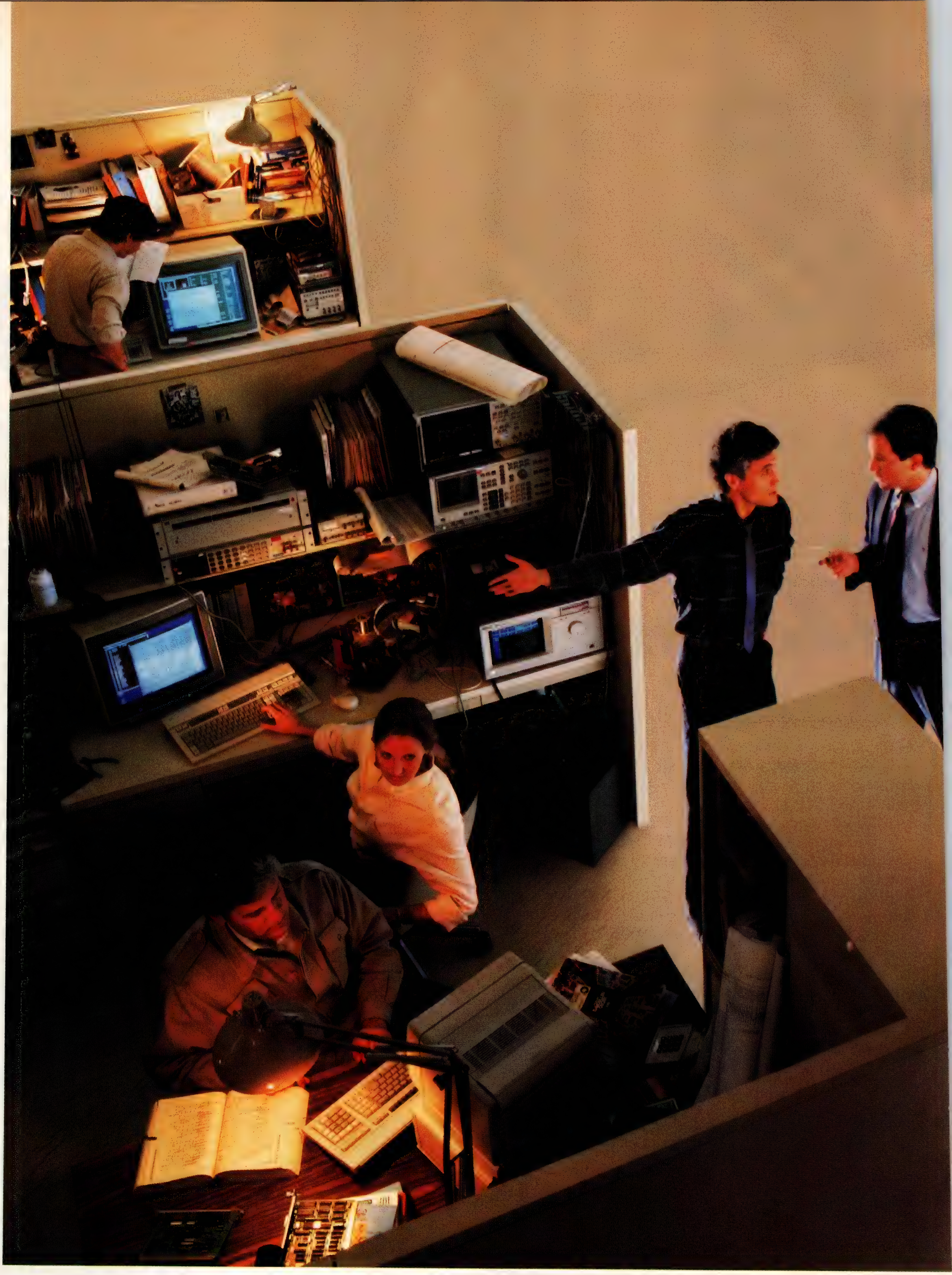

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# NEWS BREAKS

EDITED BY JOANNE DE OLIVEIRA

## LOW-COST FUNCTIONAL TESTER OFFERS MIXED-SIGNAL TESTING

To produce the Testar System 4000 desktop functional tester, Proteus Corp (Littleton, CO, (303) 795-5944) blended a Compaq personal computer, an 18-slot VME Bus rack, an assortment of standard test cards and power supplies, and a custom test head, then added a large amount of software to the PC. The test system employs guided-probe troubleshooting and shows the operator where to place the test probe by using the PC's graphics to paint a realistic picture of the circuit board under test. The tester employs Pascal for its test-programming language and includes several utility programs to help you generate, debug, and run functional tests. Yet another utility program allows you to create graphic images of the circuit boards. In operation, the tester verifies what it can from the circuit board's connectors. Next, it guides the operator to the suspect circuit nodes by superimposing a large arrow on the displayed image of the board; the arrow points to the device pin or lead in question. Because the system employs modular test cards, you can tailor the capabilities of the Testar System 4000 to your specific test needs. Prices start at $50,000.—Steven H Leibson

## VENDOR UNVEILS BOTH RISC- AND CISC-BASED WORKSTATIONS

Two months after a rival workstation vendor surprised almost everyone by making sweeping changes to its workstation product family, Sun Microsystems (Mountain View, CA, (415) 960-1300) parried the attack by making some changes of its own. In a move that could be interpreted either as hedging its bets or as serving both sides of the market, Sun announced both SPARC RISC-based workstations and 68030 CISC-based workstations. The SPARCstation 1 is a low-end workstation that provides 10 MIPS and 1.5M flops; it costs less than $10,000. The higher-end SPARCstation 300 Series uses a 25-MHz SPARC CPU to perform 15 MIPS and 2.5M flops; it costs under $30,000. Optional graphics upgrades let you use the workstations for 3-D modeling applications. The SPARCserver 330 is an entry-level server for a multiuser configuration. You can configure the 330 with as much as 1.3G bytes of disk memory and 40M bytes of main memory.

Sun offered some rays of hope for 68030 fans, too. The Sun-3/80 delivers 3 MIPS and 0.15M flops with 4M bytes of memory and as much as 200M bytes of internal disk space. Its price starts at less than $7000. The 3/470 performs 7 MIPS and 0.8M flops and costs as little as $35,000. Like their RISC-based cousins, the Sun-3 workstations offer optional graphics upgrades. Further, the Sun 3/480 servers support 14.3G bytes of disk storage and 128M bytes of main memory in a network system.
—Michael C Markowitz

## TOUCHSCREEN SENSES FINGER PRESSURE AND POSITION

Conventional resistive, capacitive, and infrared touchscreens sense finger position only. Unlike those conventional models, the Z-Touch touchscreen from Transparent Devices Inc (Westlake Village, CA, (805) 497-8500) senses pressure as well. Finger pressure on a resistive touchscreen causes a film coated with transparent vertical conducting traces to touch a film directly behind it that is coated with transparent horizontal conducting traces. Scanning electronics convert the signals from the horizontal and vertical traces to an x-y position. The Z-Touch screen has a third film, and its electronics can sense when the pressure is strong enough to press the first two films into the third. (Surface-acoustic-wave (SAW) touchscreens can also detect

finger pressure, but when two fingers press the screen simultaneously, the screen electronics gives the x-y position as the average of the two positions.) To activate the third screen, the Z-Touch requires finger pressure that's about four times the pressure required for two screens. For example, if normal pressure on the screen is 25g, you need to apply 100g to activate the third layer. The manufacturer claims the screen's life is at least 6 million cycles. A 7-in. diagonal touchscreen costs $130.—Margery Conner

### SOFTWARE PERFORMS ELECTRICAL PARAMETER EXTRACTION

Valid Logic Systems' (San Jose, CA, (408) 432-9400) Allegro Release 3.0 lets you study the potential transmission-line effects that can affect your pc boards—before the boards go to manufacturing. The interactive electrical-parameter calculator obtains measurements of expected circuit behavior such as impedance, propagation delay, capacitance, inductance, and resistance. When you know these values, you can modify your design to achieve the signal behavior you need.

Additional enhancements to Allegro include two design-rule checks (DRCs), one by component height and one by net group. With these DRCs, you can specify a maximum component height to prevent potential interference that might result from the placement of large components, and you can create net classes for variably spaced line-to-line DRCs. The Allegro 3.0 runs on the Sun-3, the Sun-4, and DEC VAXstations and DECstations. The upgrade is available at no cost to current users who have maintenance contracts; otherwise, it costs between $20,000 and $50,000, depending on the configuration.—Michael C Markowitz

### MULTIPLEXERS BOOST PERFORMANCE OF MULTIUSER SYSTEMS

Systech Corp (San Diego, CA, (619) 453-8970) now offers a second generation of its Unplug family of multiplexer products. The multiplexer family includes host adapters that occupy a single VME Bus or Multibus slot in the host computer. Eight- and 16-channel cluster controllers connect to the host via a single coaxial cable, and they can interface as many as 255 RS-232C devices to a system. (The first generation of products could serve 128 serial devices from a single host adapter.) The HPS-6200 Series host adapters range in price from $1765 to $2210 (100), and the HPS-7000 line of cluster controllers costs $858 to $1045 (100). The new family of products also includes the HPS-6236 and 6237 16-channel VME Bus multiplexer cards (the 6237 includes a parallel port). The bus-resident multiplexers cost $1185 and $1260 (100), respectively. The company achieved the new price/performance levels by designing and using a custom 8-channel UART IC called an Octart. The multiplexer family will be available in the second quarter.—Maury Wright

### STD BUS CARD MONITORS EVENTS ON 24 LINES WITHOUT POLLING

The ZT8846 event-sense interface, an STD Bus card from Ziatech Corp (San Luis Obispo, CA, (805) 541-0488) lets you monitor events on 24 lines. The board takes advantage of the STD Bus's capability of supporting cascaded interrupt controllers, a feature that's not available on the IBM PC bus. Each of the 24 lines can generate a unique interrupt vector by using a single hardware-interrupt line. These interrupts quickly signal an STD Bus processor of events or changes in status without wasting processor time on polling. The board can generate interrupts on high transitions, low transitions, or both. You can individually enable or disable interrupts in software. The card costs $495.—Doug Conner


# TMC2310 Runs 1024-Point FFT in 0.5ms

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## MODEMS CONFORM TO LATEST CCITT ERROR-CORRECTION STANDARDS

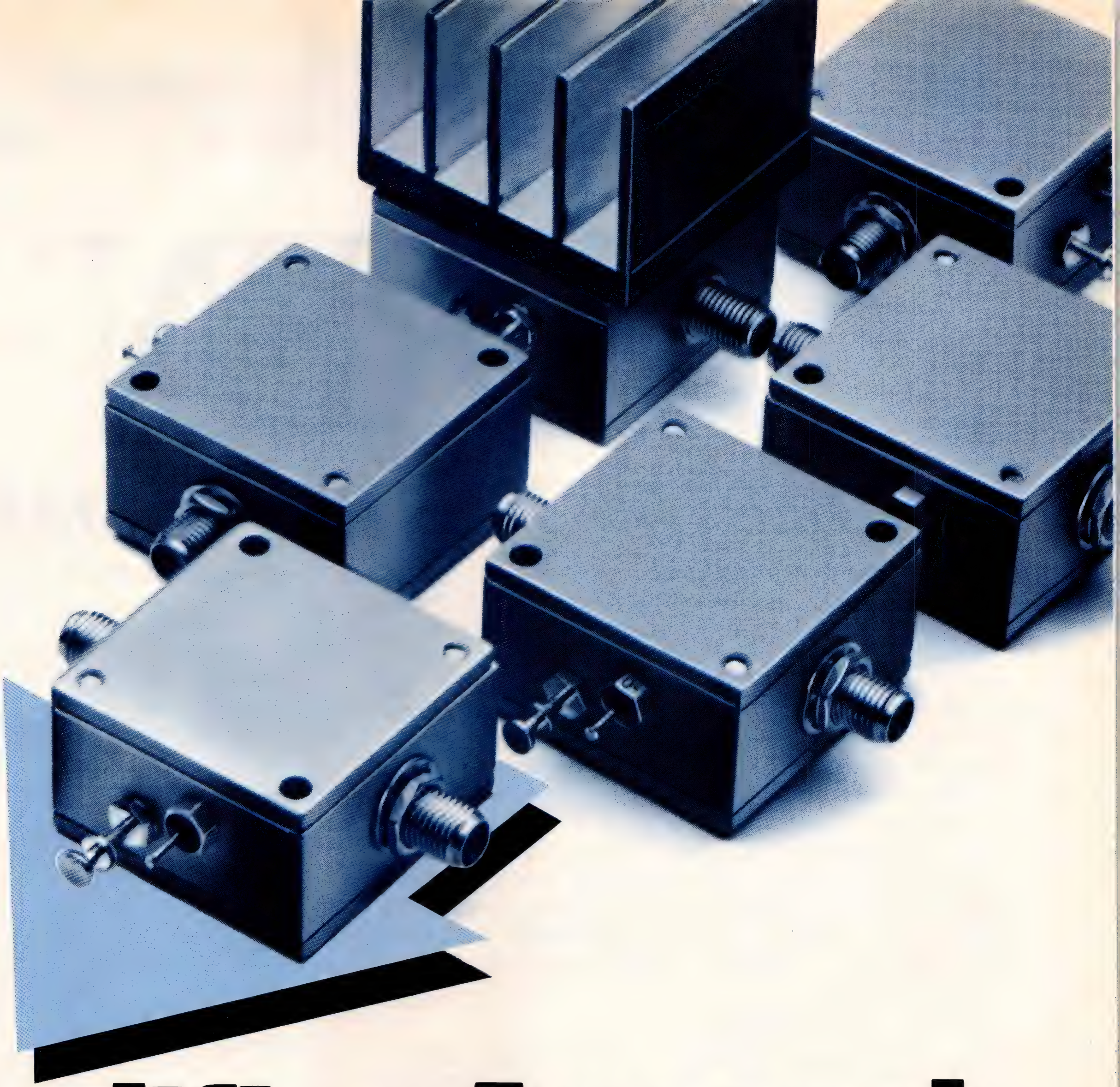
The Sprint-24QB and -96QB asynchronous dial-up modems from Mayze Systems Ltd (Swindon, UK, FAX 0793-511683) comply with the V42 standard, which is the latest error-correction standard from the CCITT. V42 is expected to become the dominant form of error correction for modems. It also implements all the requirements of the V42-bis data-compression standard. The modems also include the MNP-5 error correction scheme, which makes them compatible with a wide range of equipment. The Sprint-24QB modem, which costs £595, has V21, V22, V22-bis, and V23 operating modes; it transmits and receives data at rates between 300 and 2400 bps. The Sprint-96QB, which sells for £1295, offers the same modes plus a V32, 9600-bps mode. Both modems feature automatic baud-rate detection, 12 prestored modem setups, five different dialing methods, and password-secured data protection. They are available as stand-alone units or as plug-in cards for the company's Network-16 distributed network-management system.—Peter Harold

## 5¼-IN., ERASABLE OPTICAL DISK DRIVE STORES 644M BYTES

Developed by Hitachi Ltd (Tokyo, Japan) in cooperation with NTT, the OD112-1 5¼-in., rewritable, optical disk drive employs magneto-optic recording to store 644M bytes on an ISO-compatible disk cartridge. The drive features a 75-msec average access time and can transfer data at a 925k-byte/sec rate in burst mode to its companion formatter/controller, the OD112S. The formatter/controller board communicates with a host system through its SCSI port, and it can transfer data to the host at a burst rate of 1.5M bytes/sec. Both the drive and the formatter/controller board are available in the US from Hitachi America Ltd (San Bruno, CA, (415) 872-1902); the pair costs $5000 in sample quantities.—Steven H Leibson

## SINGLE-EUROCARD PC SUITS INDUSTRIAL APPLICATIONS

The ECPC single-board computer from DSP Design (London, UK, FAX 01-482-1779) provides you with IBM PC compatibility on a single-Eurocard pc board. The ECPC is compatible with the IBM PC at both the BIOS and the hardware-register level. Based on the NEC V40 μP, the board includes a disk controller for 3½- or 5¼-in. floppy-disk drives; an RS-232C (serial) port; a Centronics (parallel) port; keyboard- and sound-output interfaces; and a graphics controller that provides CGA, monochrome, or Hercules-compatible graphics. As an alternative to booting MS-DOS from disk, you can configure the board to boot the operating system from an onboard 128k-byte ROM disk. The board can stand alone, or you can implement system expansion via its STE Bus interface. The computer is constructed from CMOS devices and operates from a single 5V supply. A version with an extended temperature range is available. The board costs from £450 to £1150, depending on its configuration.—Peter Harold



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Need more output? Our ZFL-1000H, flat from 10 to 1000MHz, delivers +20dBm output.

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SPECIFICATIONS

| MODEL | FREQUENCY MHz | GAIN, dB (min.) | MAX. POWER OUTPUT dBm(typ) | NF dB(typ) | PRICE $ Qty. (1-9) Ea. |
|---|---|---|---|---|---|
| ZFL-500 | 0.05-500 | 20 | +9 | 5.3 | 69.95 |
| ZFL-500LN | 0.1-500 | 24 | +5 | 2.9 | 79.95 |
| ZFL-750 | 0.2-750 | 18 | +9 | 6.0 | 74.95 |
| ZFL-1000 | 0.1-1000 | 17 | +9 | 6.0 | 79.95 |
| ZFL-1000G* | 10-1000 | 17 | +3 | 12.0 | 199.00 |
| ZFL-1000H | 10-1000 | 28 | +20 | 5.0 | 219.00 |
| ZFL-500HLN | 10-50 | 19 | +16 | 3.8 | 99.95 |
| ZFL-1000LN | 0.1-1000 | 20 | +3 | 2.9 | 89.95 |
| ZFL-1000VH | 10-1000 | 20 | +25 | 4.5 | 229.00 |
| ZFL-2000 | 10-2000 | 20 | +17** | 7.0 | 219.00 |

* 30dB gain control **+15dBm below 1000MHz

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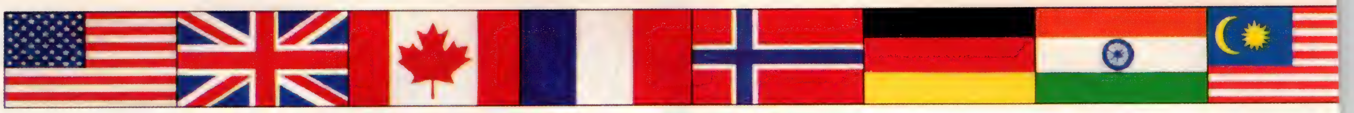
C101 REV.F



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The WREN family of 5¼" disk drives delivers the highest performance available today. For example, the WREN RUNNER™ has an average seek of only 10.7 ms. And all WREN products use a patented balanced straight-arm actuator. This reduced-mass design, unique to WREN, results in precision read/write head positioning and faster seek times.

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WREN drives feature a 40,000 hour MTBF, lower power consumption, special shock mounts, lifetime internal HDA environmental control, automatic actuator restraint and a dedicated head landing zone. It all adds up to years of trouble-free operation.

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We've made the fastest, most reliable 5¼" disk drives better than ever. The new WREN VII has a capacity of 1200 Mbytes and is available with the SCSI interface. What's more, it uses IMPRIMIS ZBR™ variable track capacity recording. ZBR offers higher capacity, performance and reliability than standard recording techniques.

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| Model | Capacity (Mbytes) (UF)/(F) | Interface | Avg. Seek (ms) | Transfer Rate (MHz) |
|---|---|---|---|---|
| WREN VII | 1200/1050 | *SCSI | 16.0 | 15-23 |
| WREN VI | 766/676 | *SCSI | 15.5 | 15 |
| | 766/676 | ESDI | 15.5 | 15 |
| WREN VI H/H | 383/338 | *SCSI | 15.0 | 18-20 |
| | 383/338 | ESDI | 16.0 | 15 |
| | 383/338 | AT | 16.0 | 15 |
| | 274/242 | AT | 16.0 | 15 |
| | 164/145 | AT | 16.0 | 15 |
| WREN V | 702/613 | *SCSI | 16.5 | 12-16 |
| | 385/339 | *SCSI | 10.7 | 15-16 |
| | 442/390 | ESDI | 16.0 | 10 |
| | 383/338 | ESDI | 14.5 | 10 |
| WREN V H/H | 209/183 | *SCSI | 18.0 | 9-15 |
| WREN IV | 376/330 | *SCSI | 17.5 | 10-15 |
| | 350/307 | *SCSI | 16.5 | 9-15 |
| WREN III | 182/160 | *SCSI | 16.5 | 10 |
| | 182/160 | ESDI | 16.5 | 10 |
| WREN III H/H | 106/94 | *SCSI | 18.0 | 10 |
| | 106/94 | ESDI | 18.0 | 10 |
| WREN II | 135/115 | RLL | 28.0 | 7.5 |
| | 96/80 | ST506 | 28.0 | 5 |
| | 86/71 | ST506 | 28.0 | 5 |
| | 85/71 | ST506 | 28.0 | 5 |
| | 86/71 | ESDI | 28.0 | 5 |
| WREN II H/H | 81/74 | AT | 28.0 | 7.5 |
| | 74/65 | AT | 28.0 | 7.5 |
| | 77/65 | RLL | 28.0 | 7.5 |
| | 51/41 | ST506 | 28.0 | 5 |

**H/H** = Half Height Models. **(UF)** = Unformatted Capacity. **(F)** = Formatted Capacity at 512 Bytes/Sector. All WREN Disk Drives have 40,000 hours MTBF. *Apple Mac compatible interface available.

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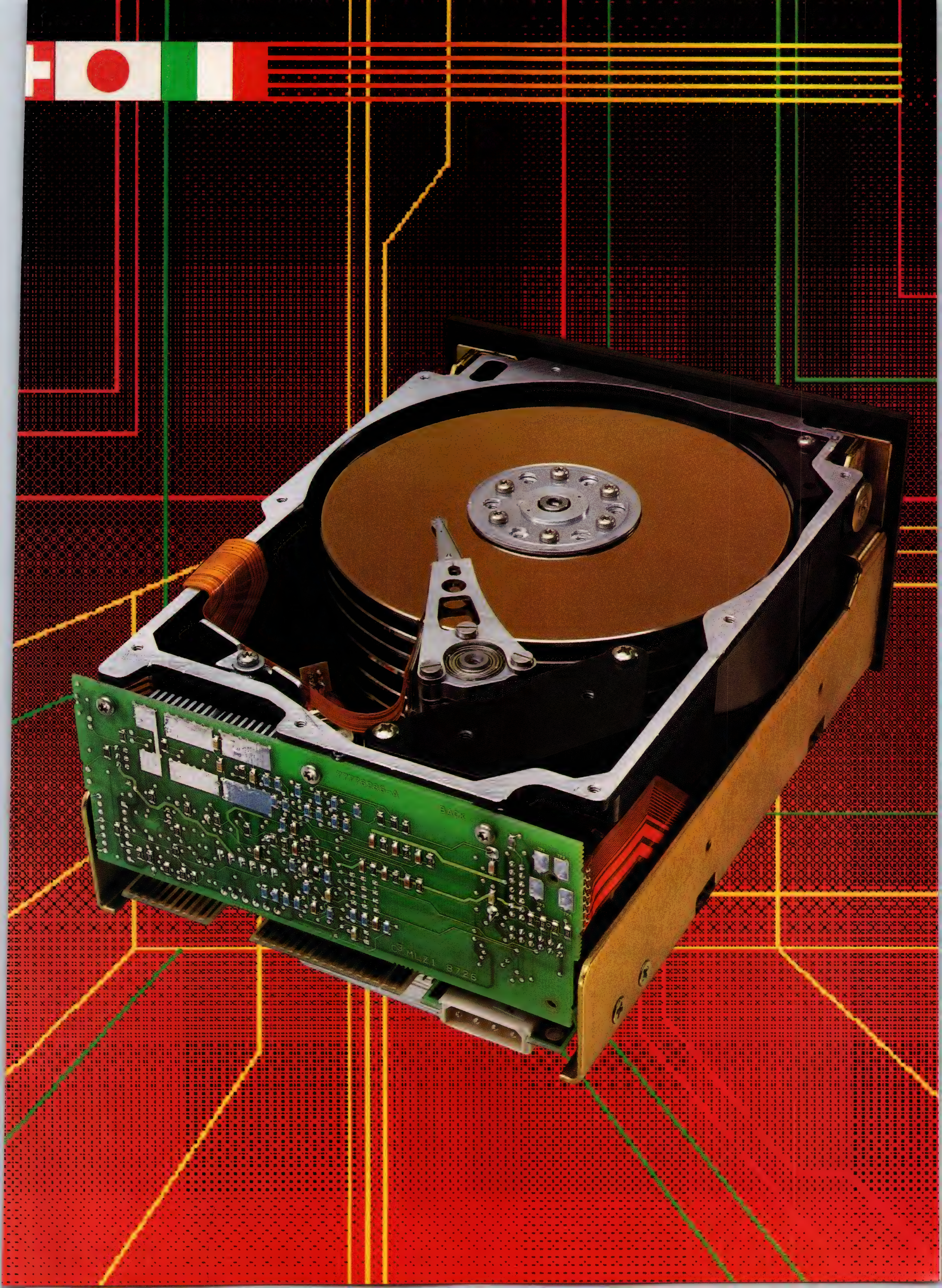
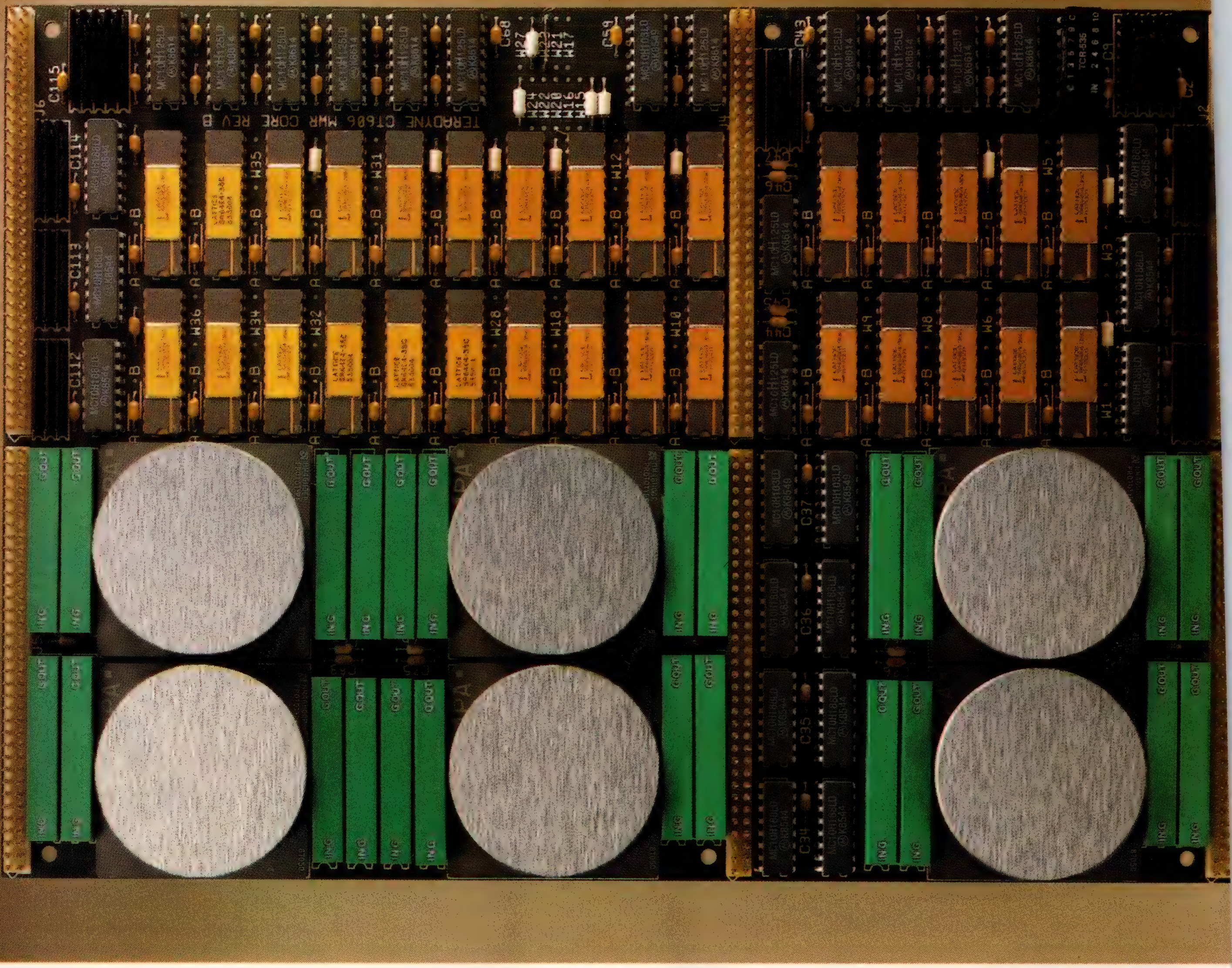
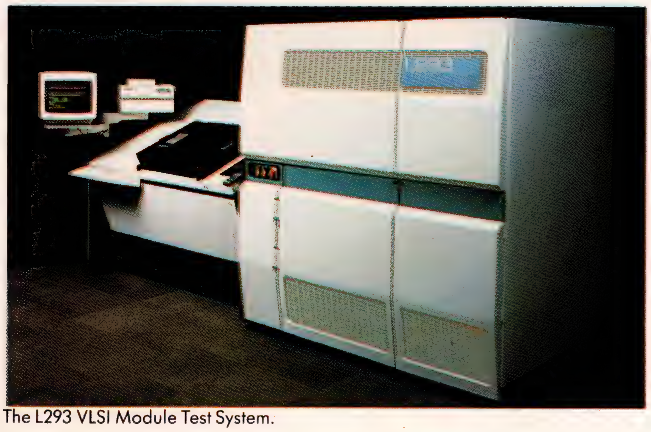




# If you're testing complex boards

You're facing one of test engineering's toughest challenges. VLSI boards like this one. But with a Teradyne L200 board tester on your side, complex test problems can be conquered quickly.



The L293 VLSI Module Test System.

**Stay in front of VLSI/VHSIC advances.**
Start with the most advanced hardware for analog and digital testing. An L200 fires functional test patterns at 40 MHz rates. At up to 1152 test channels. Top speed is 80 MHz. That's 4 to 8 times faster than any competitor can deliver.

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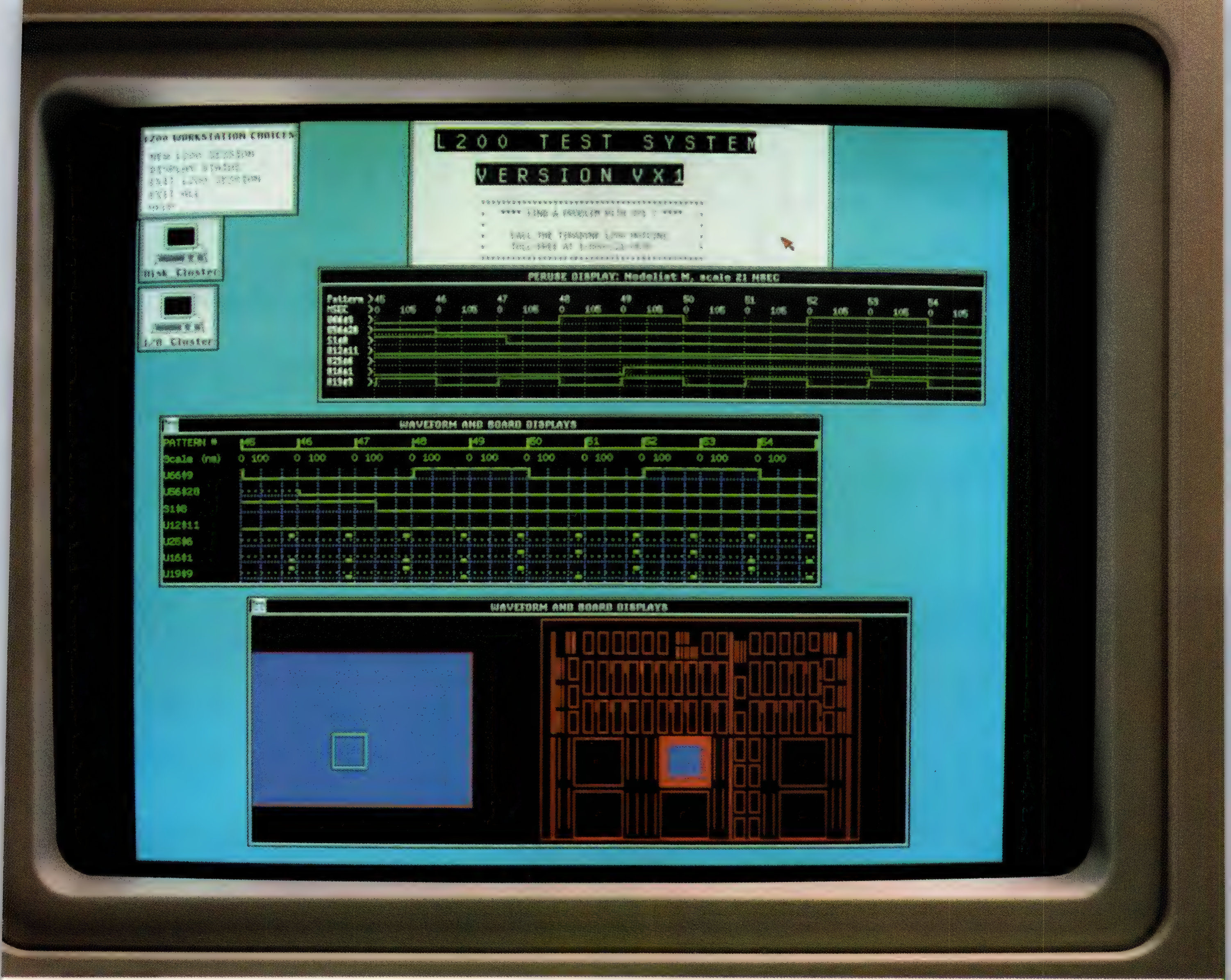
Testing is controlled by a VAX computer. It sends tasks to specialized processors for rapid deployment of analog, digital, and memory tests.


L200 TEST SYSTEM
VERSION VX1
PERUSE DISPLAY: Modellst M, scale 21 NSEC
WAVEFORM AND BOARD DISPLAYS
WAVEFORM AND BOARD DISPLAYS
Disk Cluster
I/O Cluster

# SIGNALS & NOISE

## Error magnifies the ENIAC

The article "The microprocessor's first two decades: The way it was" by James F Donohue, which appeared in EDN's Special Microprocessor Issue (October 27, 1988, pg 18), requires a correction to set the record straight. Way back when, someone made an error in dimensions that has been promulgated by numerous uninformed writers, including James Donohue. He states that "the first electronic computer, the fabled ENIAC, . . . filled 3000 cubic feet."

The statement contains not one but two major errors. Normally, the error appears as "3000 square feet"; however, your article errs in the magnitude as well as the units. The statement should read "1500 square feet." To clarify the issue properly, the computer system was in a room containing approximately 1800 square feet; the computer itself occupied 1500 square feet. The ENIAC was, of course, at the BRL (Ballistic Research Laboratory), where this computer-generated letter is being prepared. In fact, my office is in the very spot where the 1800 square feet is (I've personally measured it at least once).

I would very much appreciate seeing a correction published in EDN so the proper figures will be seen by all, once and for all! One doesn't need an ENIAC or a Cray (we have the latter now as well as a small portion of the former) to get the numbers correct.

*Michael B Danish*
*Ballistic Research Laboratory*
*Aberdeen Proving Ground, MD*

## Setting the record straight on CP/M

I enjoyed your Special Microprocessor Issue (October 27, 1988). The issue brought back memories of the "early days," but it also included an error that I have seen repeated

"DON'T BE A PUSSYCAT! TAKE THE BULL BY THE HORNS! GET TOUGH! LOOK HIM STRAIGHT IN THE EYE AND DISAGREE!—JUST DON'T TELL HIM I SAID SO."

in numerous books, magazines, and even a computer trivia game. In the article "The microprocessor's first two decades: The way it was" (pg 18), James Donohue states on pg 25 that Gary Kildall wrote a disk-based operating system and called it CP/M (Control Program/Microcomputers). The "M" did not stand for "Microcomputers," it stood for "Monitor." And "Monitor" didn't mean a CRT or "the tube."

Recall that in the early days, one had to be wealthy (or a fanatic) to own a floppy-disk drive, more than 8k bytes of RAM, or a CRT. The pioneers instead used old teletype equipment for data entry and display, and paper tape or cassette recorders for mass storage. Kildall included a program with his system that used very little memory, yet allowed the user to perform very elementary functions (clear memory, load paper tape, etc), because most users did not have floppy-disk-based systems. This program was called the "monitor."

For the sake of technical and historical accuracy, let's set the record straight: The "M" in CP/M means "Monitor."

*Jerome Johnston*
*Applications Engineer*
*Crystal Semiconductor*
*Austin, TX*

## Starts with D

The article "The microprocessor's first two decades: The way it was" (EDN's Special Microprocessor Issue, October 27, 1988, pg 18) erroneously stated that Digital Equipment Corp had teamed with Motorola to develop a 100-MIPS ECL version of the 88000 RISC processor. In fact, it's Data General that has joined with Motorola to create the processor. Data General has agreed with Motorola to build a family of products using the CMOS 88000 RISC processor, and the two companies will jointly develop the high-end ECL version, which they expect to have by 1991. Data General will design the ECL chip; Motorola will manufacture and market it. The ECL chip will be fully compatible with the CMOS 88000 chip.

## Design Idea correction

If some EDN readers found my Design Idea "Single MACD performs IIR filtering" (EDN, October 13, 1988, pg 248) a bit confusing, they have my sympathy. The second page of Listing 3, starting with line 0056, was printed at the bottom of Listing 2. The text contains numerous references to FBVEC, but there's no such symbol in any of the listings!

For the benefit of anyone who hasn't by now either figured this all out from the comments in the listings, or dismissed it as a Halloween trick, an excerpt or two from my original manuscript would be in order. Most of the gremlins got into the second paragraph. I present here the original:

"To use a single MACD loop, the feedback value must be the filter output. The two delay vectors may be concatenated in either order; the coefficients are stored in reverse order of the corresponding vector elements, since the vector is addressed in reverse order because of the DMOV operation in the MACD.

With INPVEC first as shown, the first word in FBKVEC gets overwritten by the DMOV of the last word of INPVEC and gets rewritten after the MACD loop. Likewise the word at the beginning of INPVEC, which is overwritten by the last execution of the MACD, gets rewritten next call with the new input sample."

The first paragraph on pg 252 should describe a constraint on the feedback coefficient scaling, not the feedback vector (FBKVEC) scaling. The original reads:

"There is no inherent need to scale FBKVEC and INPVEC identically. Only the feedback coefficients are constrained to scale factors which can be shifted with available P modes and output shifts to keep the total shift from FBKVEC back to itself zero."

Two other, less confusing, errors also appeared. The word "bit" was added after "ARP" in the first paragraph. The ARP (Auxiliary Register Pointer) has three bits. Finally, the last paragraph contains a sentence that begins: "Note also that the routine executes the low-order filter section in reverse order . . . ." The word "section" should be plural; that is, the last filter section is executed first.

*Richard H Neubert*
*Miltope North*
*Springfield, VT*

## Wish granted

In response to David Cockerell's "μP/memory wish list" in the Signals & Noise column of EDN's October 13, 1988, issue (pg 33), David need only look to National Semiconductor's Series 32000 family of 32-bit microprocessors. Both the NS32532 and the NS32332 microprocessors feature dynamic bus sizing, which lets the CPU accommodate 8-, 16-, or 32-bit-wide buses.

The company also offers a trio of dynamic-RAM (DRAM) controllers, the DP8420A/21A/22A, that make interfacing to DRAM as easy as interfacing to static RAM. These devices are software programmable to work with all popular microprocessor families.

*Jeffrey Goldberg*
*Series 32000 Applications Engineer*
*National Semiconductor*
*Santa Clara, CA*

### WRITE IN

Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.



CIRCLE NO 1

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SCRAMs are Static CMOS Random Access Memories from Performance Semiconductor. At 15ns address access time these 64K's and 16K's are the world's fastest. SCRAMs are manufactured in Performance's six inch class 1 fabrication facility using PACE II 0.7 micron gate length technology which has set the standard for memory speed.

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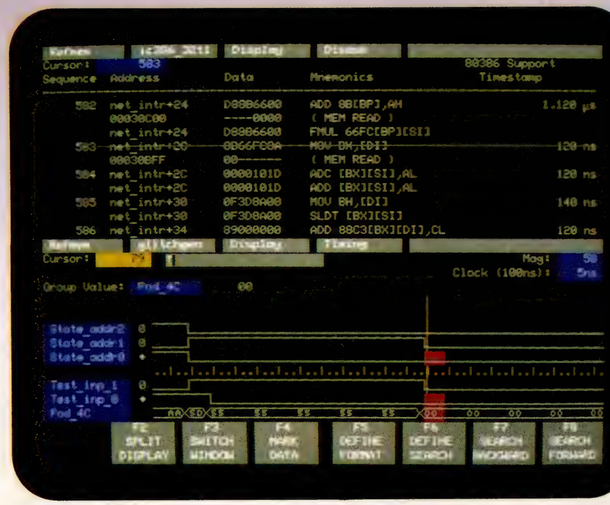

Split screen display of data acquired simultaneously from two microprocessors. The cursors can be locked to scroll in parallel, highlighting data nearest to the same point in time.

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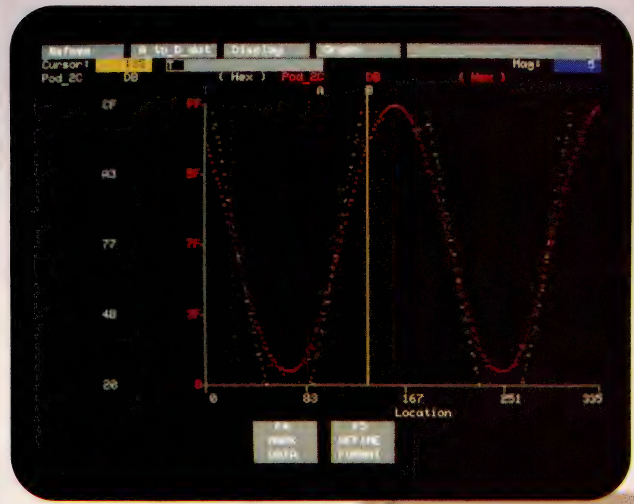
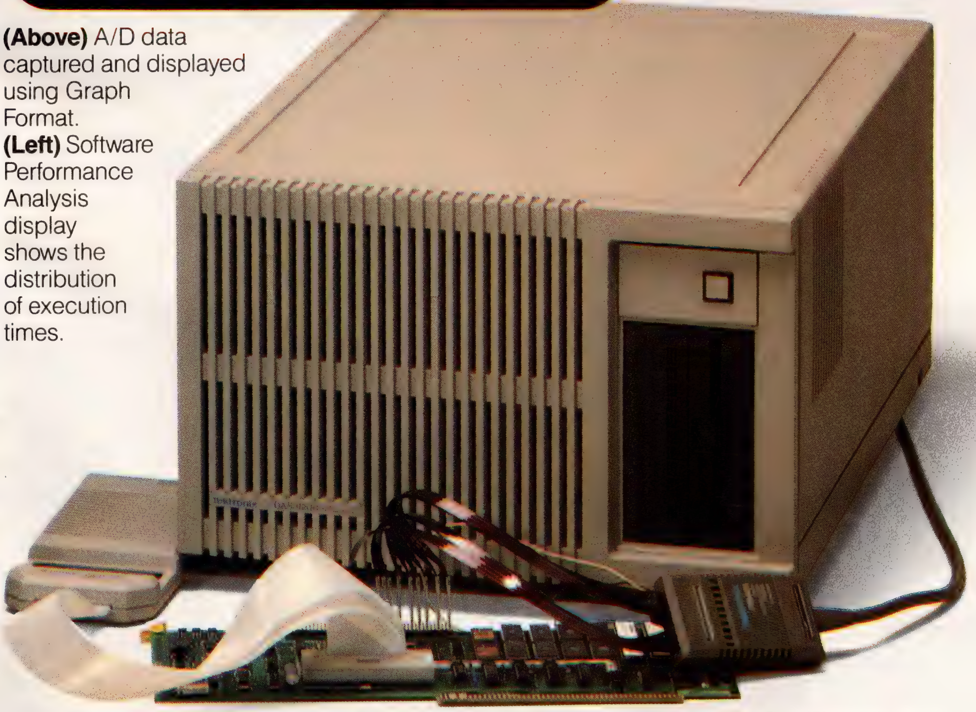
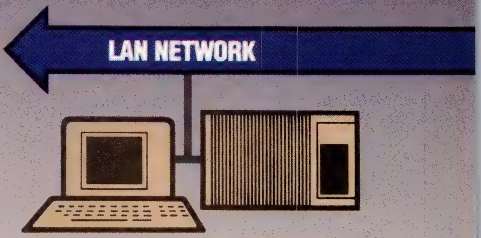


**(Above)** A/D data captured and displayed using Graph Format.
**(Left)** Software Performance Analysis display shows the distribution of execution times.

## 2 GHz

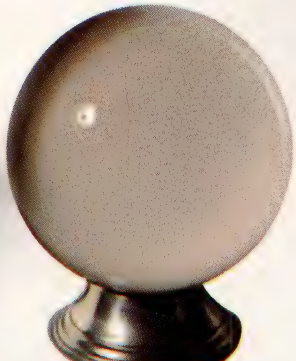
For applications requiring nanosecond edge resolution, the 92HS8 High-Speed Timing Module gives you 2 GHz bandwidth and a 500 ps sample interval, supported by a <1 pf input capacitance probe that eliminates common-mode noise and circuit loading. The 92HS8 also welds together to serve wide, parallel applications with no width/speed tradeoffs.




One new asked-for option is the 92LAN card, allowing the DAS to act a network node for efficient file transfer.

Add in its new 8 MB memory for fast response, new 40 MB hard disk, standard, and an assortment of software enhancements, and you see that the DAS not only started in a league by itself. It's staying there.

To find out more about the DAS 9200, contact your Tek representative, or call 1-800-245-2036. In Oregon, 231-1220.



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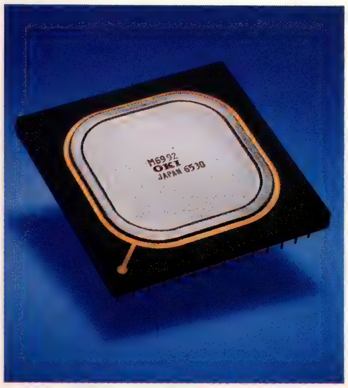

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# CALENDAR

**Modern Electronic Packaging** (seminar), Baltimore, MD. Technology Seminars Inc, Box 487, Lutherville, MD 21093. (301) 269-4102. April 18 to 20.

**12th Annual IEEE Design for Testability Workshop,** Vail, CO. T W Williams, IEEE Subcommittee on DFT, IBM Corp, Box 1900, Boulder, CO 80302. April 18 to 21.

**DOD-STD-2167A/2168** (seminar), Orlando, FL. David Maibor Associates, Box 846, Needham Heights, MA 02194. (617) 449-6554. April 24 to 25.

**American Power Conference,** Chicago, IL. Robert W Porter, Illinois Institute of Technology, Chicago, IL 60616. (312) 567-3202. April 24 to 26.

**The Computer-Aided Software Engineering Symposium (CASES),** Boston, MA. Elizabeth C Barnaby, Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 475-6990. April 24 to 26.

**Advanced Microprocessor Troubleshooting Techniques** (seminar), Dayton, OH. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (913) 898-4695. April 25 to 27.

**Local Area Networks: Implementation and Configuration** (short course), College Park, MD. University of Maryland University College Center for Professional Development, University Blvd at Adelphi Rd, College Park, MD 20742. (301) 985-7122. May 2 to 4.

**Improved Reliability Through Environmental Stress Screening** (seminar), Milwaukee, WI. John T Snedeker, Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth St, Milwaukee, WI 53203. (414) 227-3120. May 3 to 5.

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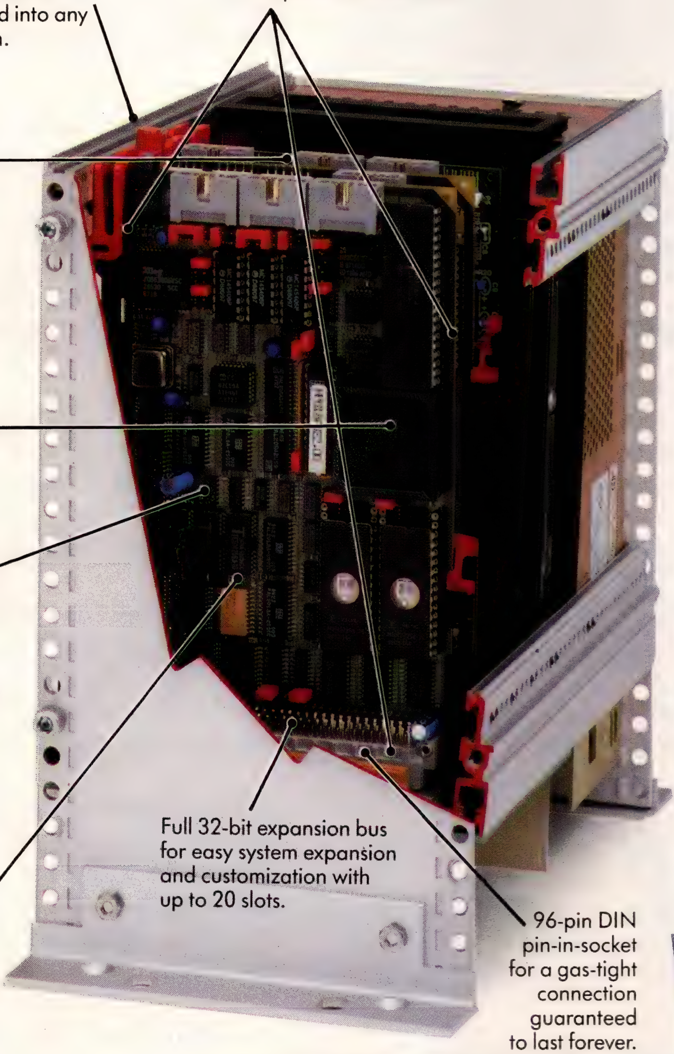


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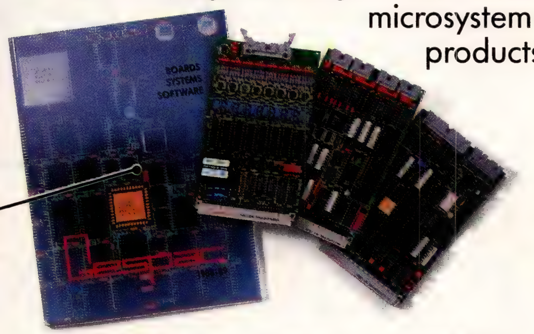


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# CALENDAR

**Fiber Optics in Local Communications** (seminar), Cincinnati, OH. Raycom Systems Inc, 6395 Gunpark Dr, Boulder, CO 80301. (800) 288-1620. May 9.

**Modern Electronic Packaging** (seminar), Chicago, IL. Technology Seminars Inc, Box 487, Lutherville, MD 21093. (301) 269-4102. May 10 to 12.

**International Symposium on Measurement Technology and Intelligent Instruments,** Wuhan, Hubei Province, People's Republic of China. Dr. Shawn Buckley, Cochlea Corp, 985 Timothy Dr, San Jose, CA 95133. (408) 920-2650. May 15 to 17.

**Custom Integrated Circuits Conference,** San Diego, CA. Marc Hartranft, Cypress Semiconductor, 3901 N First St, San Jose, CA 95134. (408) 943-2681. May 15 to 18.

**Hands-On Unix for Programmers** (short course), Seattle, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 527-3385. May 17 to 19.

**CASE Benchmarks: A Seminar Comparing Leading CASE Tools,** Toronto, Ontario, Canada. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 470-3880. June 5 to 7.

**Troubleshooting Microprocessor-Based Equipment and Digital Devices** (seminar), Portland, OR. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (913) 898-4695. June 13 to 16.

**ATE & Instrumentation Conference East,** Boston, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. June 19 to 22.

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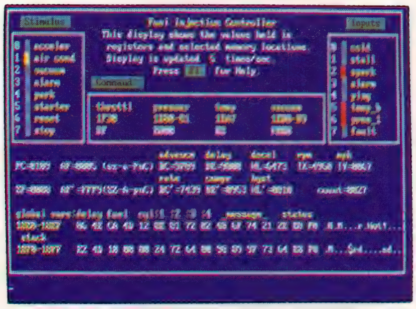

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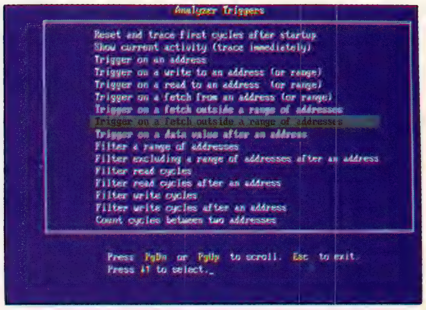

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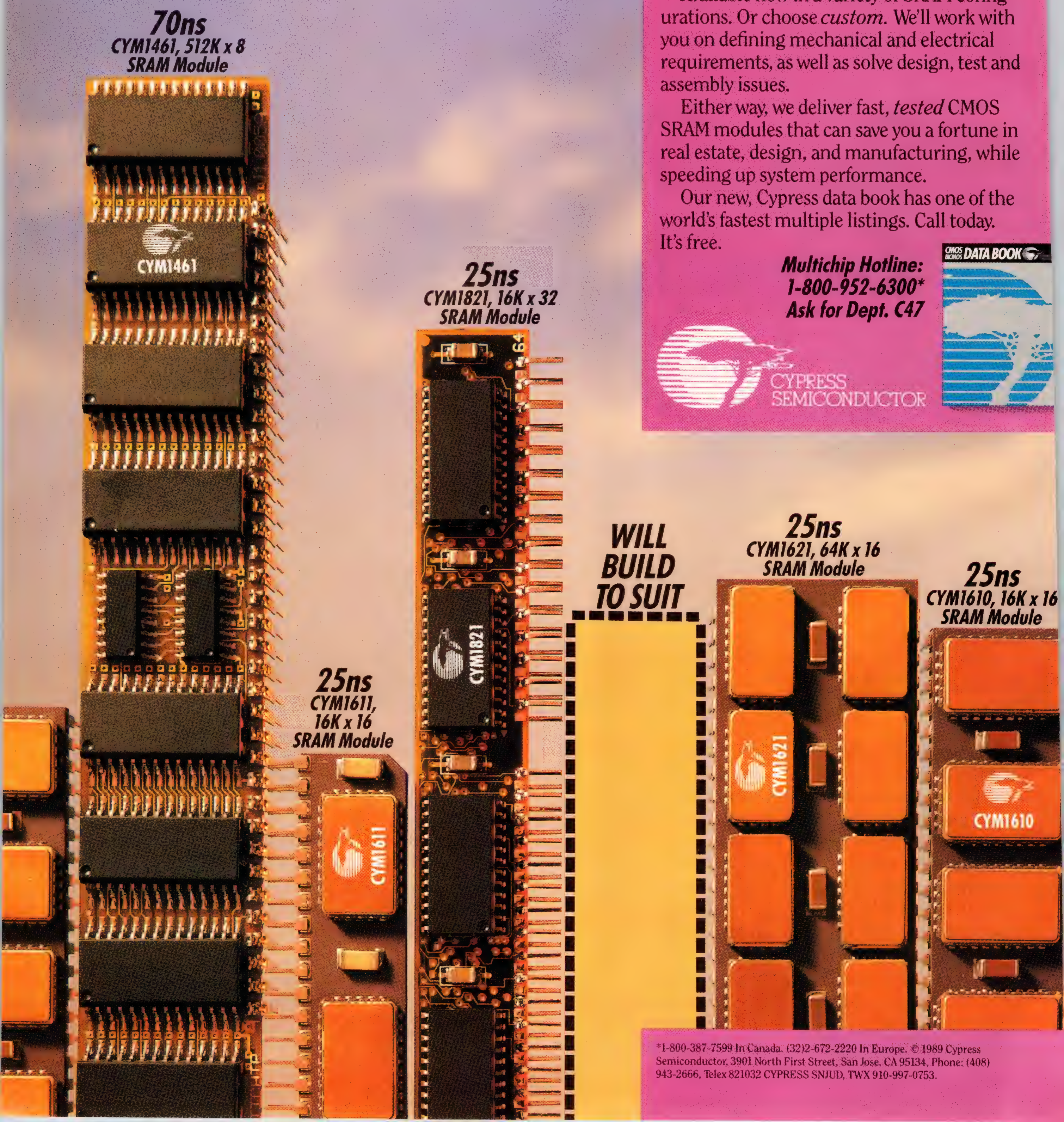


*1-800-387-7599 In Canada. (32)2-672-2220 In Europe. © 1989 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134, Phone: (408) 943-2666, Telex 821032 CYPRESS SNJUD, TWX 910-997-0753.

# Free the Mario Brothers

Suppose for a minute that an electronics company sets out to capture a large share of the small-computer market. To do so, it designs and builds a computer that is superior to anything else available. The company's share of the market grows, but software suppliers find that the computer's architecture prevents them from independently developing programs for the computer.

In order to sell their programs, the software suppliers must first submit the programs to the computer manufacturer, which accepts them or rejects them. If the manufacturer accepts a program, it extracts an exclusive license from the software developer, manufactures the program itself, and finally sells it back to the developer. Only then can the software developer put the program on the market.

If the situation above seems implausible to you, you haven't kept up with the new video games. Nintendo of America, a manufacturer of popular video games such as Contra and the Super Mario Brothers, has been using just such a strategy to lock up about 80% of the video-game market in the US. Until recently, Nintendo has controlled 100% of the add-in market for compatible game cartridges. Nintendo exerts control by incorporating a proprietary lock-out chip that prevents the use of "unauthorized computer software" in the game unit.

By applying reverse-engineering techniques, Atari Games Corp and Tengen Inc recently came up with a method that obviates the Nintendo security chip, and they began to market games for the Nintendo system without first obtaining Nintendo's approval. Atari Games also filed an antitrust suit against Nintendo. Instead of meeting the competition head-on, Nintendo countersued, claiming, among other things, that a patent covers the lock-out chip.

Nintendo also claims that the lock-out chip promotes quality software—which only Nintendo may judge—while simultaneously preventing an over-supply of game cartridges, which Nintendo also controls. Keep in mind that in Japan, Nintendo's games don't require a lock-out chip, because, according to Tengen, Nintendo already claims 90% of the Japanese video-game market. Why spend money on an extra chip when you own the market?

Clearly, Nintendo's efforts seem to be aimed at securing control of the US video-game market. Despite the institution of the patent—which was intended to protect inventors' rights, not to confer a monopoly on any one company—the use of technology to protect markets and establish a monopoly hurts suppliers, hurts customers, and hurts the electronics industry. Years ago, the courts told large computer companies that they couldn't force buyers to purchase bundled hardware and software from one source. Likewise, copier companies were told that they couldn't force customers to buy supplies from only one source. Nintendo should take a close look at those lessons, and use technology to compete, not to monopolize.

**Jon Titus**
**Editor**


Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

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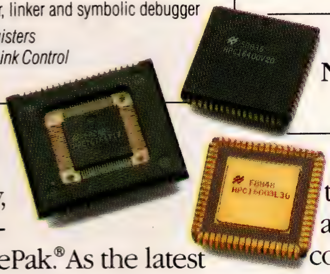
HPC PRODUCT FAMILY SUMMARY

| Part # | 16-bit Timers | UPI | I/O | Memory ROM | Memory RAM | Features |
|---|---|---|---|---|---|---|
| HPC16003* | 8 | Yes | 32 | 0 | 256 | 4 ICRs |
| HPC16004 | 8 | Yes | 32 | 0 | 512 | 4 ICRs |
| HPC16064 | 8 | Yes | 52 | 16K | 512 | 4 ICRs |
| HPC16083* | 8 | Yes | 52 | 8K | 256 | 4 ICRs |
| HPC16104 | 8 | Yes | 32 | 0 | 512 | 8 CH A/D |
| HPC16164 | 8 | Yes | 52 | 16K | 512 | 8 CH A/D |
| HPC16400 | 4 | No | 52 | 0 | 256 | 2 HDLC & 4 DMA |
| HPC16083MH | 8 | Yes | 52 | 8K UV | 256 | UV Emulator |

Standard features: Watchdog, Synchronous Serial Peripheral Interface, Uniform Memory Address Space, UART, 32X16-bit divide, 16X16-bit multiply, and available as standard cell.

DEVELOPMENT TOOLS:
- PC-based development system
- Relocatable C compiler, linker and symbolic debugger

*ICRs = Input Capture Registers*
*HDLC = High-Level Data Link Control*
**MIL-STD 883C*



Another is packaging, and specifically, our unique feature called TapePak.® As the latest generation in VLSI packaging, TapePak gives you a wide variety of industry-standard, high-density, high-leadcount options. When you put it all together, then throw in eight timers and up to 11 addressing modes, you can easily see why members of the HPC family are considered smart cookies indeed.

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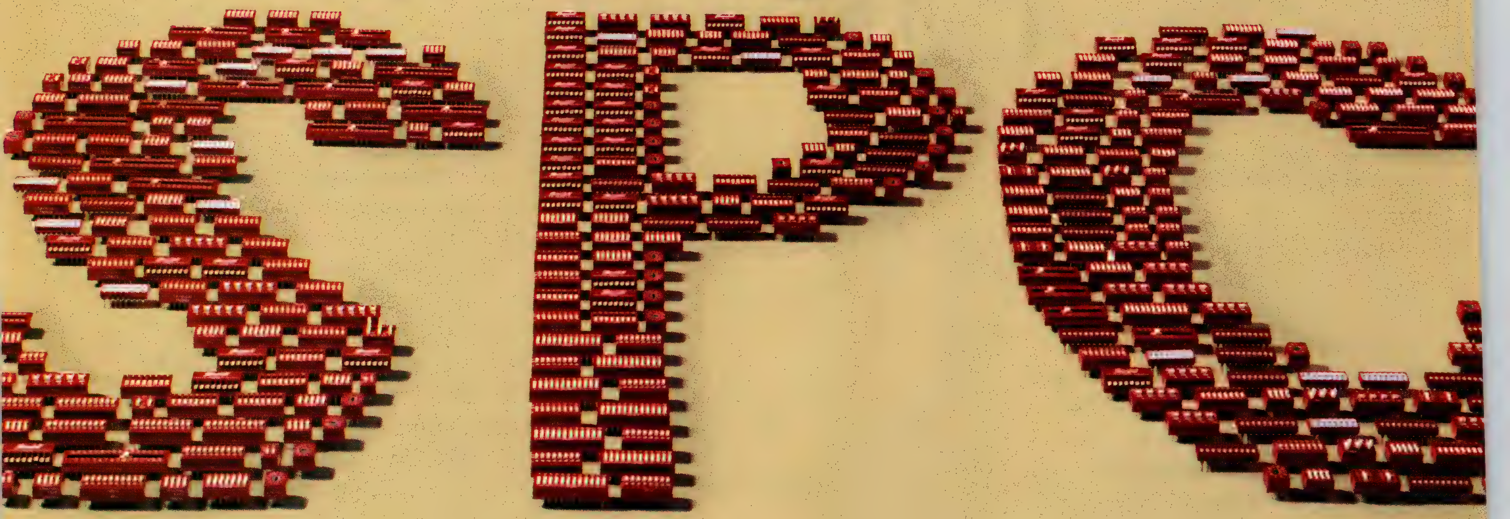
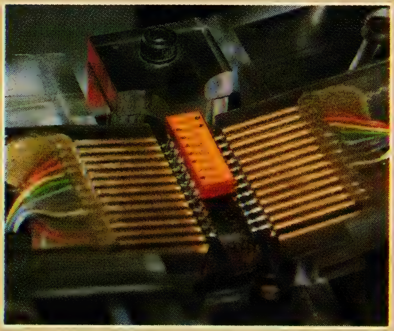
CIRCLE NO 58

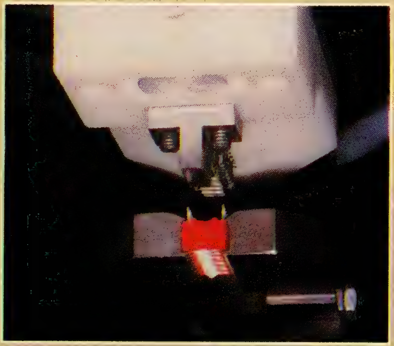
# Grayhill Statistical Process Control makes DIP switch quality a reality, not a slogan



## Is *your* DIP switch supplier being measured by SPC?



*Grayhill DIP Switches are tested every step of the way in the manufacturing process. If initial contact resistance varies from control limits, the problem is immediately diagnosed and cured.*



*This machine automatically tests every DIP switch for actuation force. We get reliable ppm data and you get reliable DIP Switches.*

The industry's reliance on Grayhill leadership has received another boost with the implementation of SPC manufacturing techniques to our DIP switch lines. (Note: SPC data not yet available for all configurations.)

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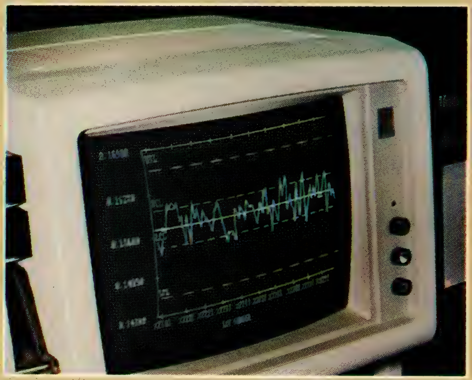

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GRAPHING-SOFTWARE PACKAGES

# Draw your graphs on printers and plotters

Your computer can plot anything you can plot by hand—usually much better and faster.

*Jon Titus, Editor*

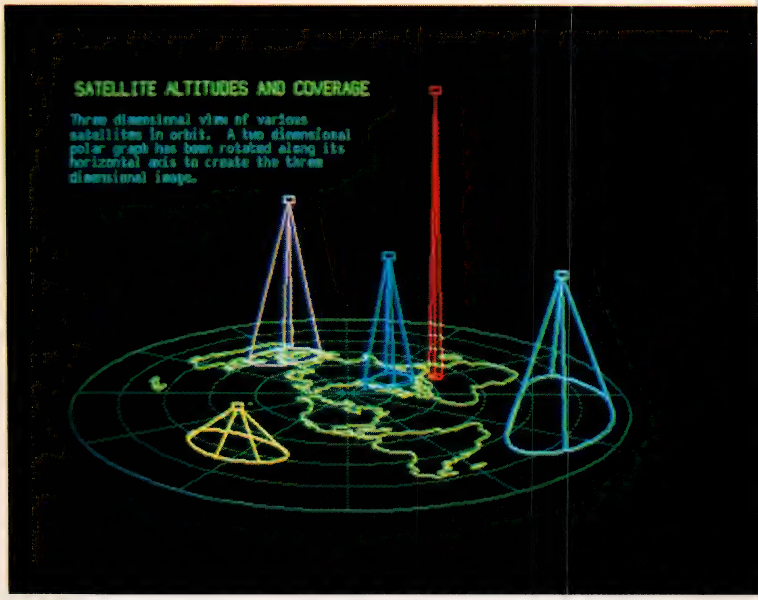
Throw away your graph paper, pens, and press-on letters. Today's small computers, when combined with a pen plotter, an ink-jet printer, or even a dot-matrix printer, let you plot almost any numerical information. Whether you plot simple 2-D x-y information or require sophisticated surface plots with hidden lines, there are software packages that can do the job for you. In fact, you can choose from two main types of graphing software—stand-alone packages and add-in graphing routines. The stand-alone packages let you plot graphs from data that you've collected and saved on paper or on a disk. The add-in routines come in handy when you're developing a computer program that requires graphing capabilities.

The selection of available graphing software reflects the popularity of their respective host computers. It's no surprise that the IBM PC family and its compatible clones lead the pack for general-purpose engineering work. Thus, all but one of the stand-alone graphing packages run on IBM PC family or compatible computers. Several of the stand-alone packages also run on Apple Computer's line of Macintosh computers or on popular workstations.

In general, all the stand-alone graphing-software packages work the same way; they let you take information from a source—usually a disk file—and then plot the data as a graph. You can display the information on your computer's monitor, or you can create a hard copy on a dot-matrix or laser printer. The packages also control a variety of plotters **(Table 1)**. The graphing-software packages control too many types of printers and plotters to list in a table. Peruse each supplier's data sheets to find out what devices each software package controls.

### Put graphs in reports

Most of the stand-alone packages also let you store a graphic image of your plot on disk. By storing an image, rather




***A typical 3-D color graph** shows how communication satellites cover various portions of the Earth's surface. It takes time and effort to learn how to create complex graphs such as this. (Courtesy 3-D Visions)*

than numerical data, you can incorporate your graph directly into a manual or a document when you're working with a word processor. You don't need to get a hard copy of your graph and then paste it into the final version of the text. Check your word processor's manual to determine which graphics-file formats it accepts.

Obviously, your graphs require information—the results of your experiments, tests, etc. The packages obtain data from several different sources. All of the stand-alone programs let your computer read data from external files that arise from data-acquisition programs, spreadsheets, or even other computer programs. All the programs also let you enter data from your keyboard.

You'll find that each of the programs provides an internal data editor, which lets you examine your information in traditional columnar form. If you're already familiar with spreadsheet programs, you'll quickly navigate your way through such editor programs. In most cases, the editors aren't fancy, but they do let you remove useless data, add new data, modify values, and so on.

An editor also comes in handy when you need to graph a few values that you've jotted on scrap paper. You start the program, type in the information, and create a graph. The editor lets you put your typed-in data into a disk file for later use.

### Dump useless data

A good data editor also lets you remove large blocks of information from your data file. For example, if you're acquiring a transient signal by using an A/D-converter board, much of what's in your file may be useless baseline-voltage values. The ability to plot the acquired signal quickly lets you locate the transient among all the baseline data. You can then use the editor to remove the baseline information so the resulting graph shows the transient without the extraneous points. (If this application is typical of what you'll be doing, you may want the ability to quickly plot every second, fifth, or tenth data point so you can see what you have in your file.)

Data editors run the gamut from simple to complex. The basic editors in PCPlot and Graphstar require about five pages of instructions to explain how they work. At the complex end of the spectrum

## TABLE 1—STAND-ALONE GRAPHING-SOFTWARE PACKAGES

| COMPANY | PRODUCT | PRICE | HOST COMPUTER | MAXIMUM DATA SET | DATA EXPORT FORMATS |
|---|---|---|---|---|---|
| BINARY ENGINEERING | TECH*GRAPH*PAD (3.1) | $395 | IBM PC, APOLLO 3000/4000, DEC VAXSTATION | 32,000 DATA PAIRS | ASCII, PIC |
| BV ENGINEERING | PCPLOT (3.25) | $125 | IBM PC, MACINTOSH | 1000 POINTS/FILE | ASCII |
| EDMOND SOFTWARE | SEGS (2.0) | $195 | IBM PC FAMILY | 11 COLUMNS× 7500 POINTS | ASCII |
| GOLDEN SOFTWARE | GRAPHER (1.77) | $199 | IBM PC FAMILY | 32,000 POINTS | NONE |
| | SURFER[1] (4.01) | $499 | IBM PC FAMILY | 16,000 POINTS | (SEE NOTES) |
| MIHALISIN | TEMPLEGRAPH[2] (3.2) | $395 | IBM PC-AT OR 80386 COMPATIBLES (SEE TEXT) | 2048 POINTS (SEE NOTES) | ASCII |
| REBUS DEVELOPMENT | PARAMETER-MANAGER PLUS (3.0) | $595 | MACINTOSH FAMILY | 32,767 POINTS/ VARIABLE | ASCII |
| SCIENTIFIC SOFTWARE SOLUTION | GRAPHSTAR (2.0) | $99 | IBM PC FAMILY | 2100 POINTS | ASCII |
| SYSTAT | SYGRAPH (1.0) | FROM $495 | IBM PC FAMILY MACINTOSH FAMILY (SEE TEXT) | 2000 POINTS | WKS, DBF, DIF, ASCII |
| 3-D VISIONS | GRAFTOOL (2.0) | $495 | IBM PC FAMILY | 14,400 POINTS (SEE TEXT) | DIF, ASCII |

KEY:
ASCII = STANDARD NUMERIC FORMAT IN ASCII CHARACTER SET
CGM = COMPUTER GRAPHICS METAFILE FORMAT
DBF = DBASE DATABASE FILE FORMAT
DIF = DATA INTERCHANGE FORMAT
DMPL = HOUSTON INSTRUMENTS COMMAND-SET FILE
DXF = AUTOCAD DATA FILE FORMAT
EPS = ENCAPSULATED POSTSCRIPT FILE FORMAT
GEM = DIGITAL RESEARCH GRAPHICS FILE FORMAT
GKS = GRAPHIC KERNEL SYSTEM
HPGL = HEWLETT-PACKARD GRAPHICS-LANGUAGE FILE FORMAT
PCX = PC-PAINTBRUSH BIT-MAPPED FILE FORMAT
PIC = LOTUS GRAPHING FILE FORMAT
TKF = TEKTRONIX GRAPHICS FILE FORMAT
WKS = STANDARD LOTUS 1-2-3 (1A) FILE FORMAT
WK1 = STANDARD LOTUS 1-2-3 (2.0) FILE FORMAT

AS = AUTOMATIC SCALING
MS = MANUAL SCALING
R = ROTATE
Z = ZOOM

lies the editor in Sygraph; it comes with a 114-page manual.

As you review the specifications for the stand-alone packages, you should also pay attention to how many values the editor can handle. For example, the Graphstar editor lets you work on a maximum of 200 values at a time. Sygraph's editor, on the other hand, can handle as many as 256 *variables* simultaneously. If the editors that you evaluate don't suit your needs, keep in mind that most programs let you exchange information with popular spreadsheet programs.

**Programs offer variety**

Like their editors, the stand-alone graphing packages cover the spectrum from simple to complex. If you need only a few x-y or logarithmic (log-log and semilog) graphs or if you routinely plot the same types of simple graphs, the packages priced below $200 will meet your needs. Thus, graphs and plots for your notebook or for internal engineering reports will be easy to produce with either PCPlot or Graphstar.

The PCPlot package provides a simple data editor and produces plots with as many as 1000 points. Unlike the other stand-alone graphing programs, PCPlot needs your computer's internal screen-print or screen-dump utility program to produce graphs on your printer. BV Engineering can supply such a utility. BV Engineering also offers PDP, a PCPlot-like program that puts graphic information on plotters. The company supplies drivers for many plotters. Unfortunately, BV Engineering's programs don't let you store graphic images in files for later use.

| GRAPHIC EXPORT FORMATS | GRAPH TYPES | GRAPH MANIPULATIONS |
|---|---|---|
| HPGL, PIC | 2-D, POLAR, LOG | AS, MS |
| NONE | 2-D, BAR, LOG, ERROR BAR | AS, MS |
| HPGL, PIC | 2-D, BAR, LOG | AS, MS, R |
| PIC, DXF, POSTSCRIPT | 2-D, LOG | AS, MS |
| HPGL, PIC, DXF, POSTSCRIPT[3] | 2-D, 3-D, BAR, SURFACE, CONTOUR | AS, MS, R, Z |
| CGM, HPGL | 2-D, POLAR, BAR, LOG | AS, MS, R, Z |
| PIC | 2-D, LOG | AS, MS, Z |
| NONE | 2-D, LOG | AS, MS |
| CGM | 2-D, 3-D, POLAR, BAR, LOG, SURFACE, CONTOUR | AS, MS, R, Z |
| HPGL | 2-D, 3-D, POLAR, BAR, LOG, SURFACE, SPHERICAL, SMITH, CONTOUR | AS, MS, R, Z |

NOTES:
1. SURFER CAN PUT EXTERNAL ARRAYS IN THE USER'S PROGRAMS.
2. TEMPLEGRAPH EDITOR HANDLES AS MANY AS 10 GRAPHS AND AS MANY AS 2048 POINTS PER GRAPH.
3. POSTSCRIPT IS A STANDARD FORMAT FOR LASER PRINTER FILES.

If you need to plot more than 1000 points, consider Graphstar, which plots as many as 2100 points. However, remember that its editor has an upper boundary of 200 data points. Don't try to edit a longer file; Graphstar truncates your data to the first 200 values. That may be a difficult limit to adapt to if you're doing complex engineering work. Unlike PCPlot, Graphstar controls dot-matrix printers as well as plotters that accept HPGL commands. However, when plotting on a dot-matrix printer, Graphstar has a painfully long printing time.

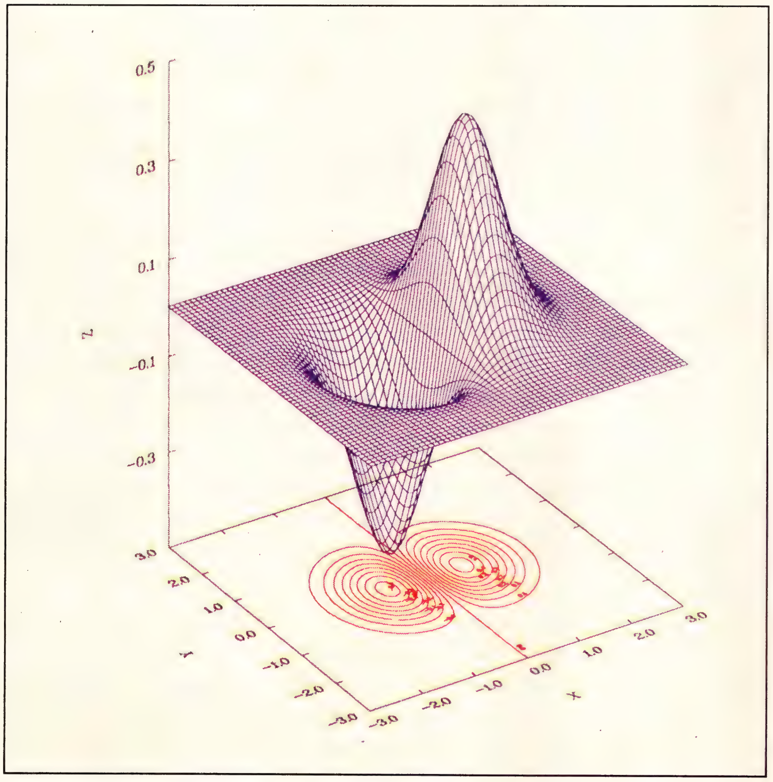
Editors, printing speeds, and file limits are important specifications to consider when you evaluate graphing software. There's another factor you should watch out for, too: missing values. First, though, you have to know what a missing value is. Assume that you're measuring current through a circuit as you apply voltages in 0.1V steps. If you take 55 readings from 0.1 to 5.5V and graph them, any graphing package can handle the job. If you can't take a reading at one or more of the voltage steps and those voltages are still listed in your table or spreadsheet, you have what are called missing values:

| | |
|---|---|
| 3.3V | 1.67A |
| 3.4V | 1.69A |
| 3.5V | |
| 3.6V | 1.78A |
| 3.7V | |

Typically, a business-type spreadsheet program plots missing values as zeros. For the data above, the current plot goes from 1.69 to 0V and back up to 1.78V. Such a graph is useless.

Graphing programs should automatically treat missing values as though they don't exist. Thus, for the data above, the graphing pro-

**Graphing-software packages**




***Combining a 3-D surface plot and a 2-D contour map*** *lets you show the same information two ways. Most of the sophisticated stand-alone graphing packages let you produce this type of effect. You can also overlay two graphs to produce a similar combination of 2- and 3-D effects. (Courtesy Systat)*

gram should ignore the 3.5 and 3.7V points. Unfortunately, both PCPlot and Graphstar treat missing values as zeros. If a program can't ignore missing values, you'll have to use the editor to remove them. That's an annoyance you may wish to live without.

**Add more capabilities**

Edmond's Scientific & Engineering Graphic System (SEGS) and Golden Software's Grapher form the next tier of graphing packages. Both furnish standard x-y and log graphs and support many printers and plotters. The packages give you a large choice of line widths and a variety of letter and number sizes for legends.

If your information requires a bit of preprocessing before you can plot it, consider the SEGS program. This program includes 19 mathematical operations that let you scale, offset, or otherwise manipulate your file prior to plotting. Keep in mind, however, that the spreadsheet accepts only numerical data. It's up to you to keep track of the headings for the various columns of figures you're working on. The program *does* keep track of axis information and labels for you. (Edmond expects to announce an enhanced version of SEGS around the time this article appears.)

Sometimes, a nice neat plot of your data may not be enough to tell you what you're looking at. So, both SEGS and Grapher let you fit your data to a curve. If a linear fit is all you need, SEGS plots the best straight-line fit through your data. When you need a closer approximation, Grapher lets you choose from six types of curve-fitting operations: linear, log, power, exponential, cubic-spline, and polynomial. Grapher also gives you the coefficients for the curve-fitting equation.

These days, engineers don't live by IBM PCs alone. If you're a Macintosh user, Rebus Development's Parameter Manager Plus software may meet your plotting needs. However, paying $595 for a program that draws only x-y and log graphs may be difficult to justify unless you also use the software's statistical, data-management, and other sophisticated capabilities. Among the extra features is the ability to handle complex numbers.

Parameter Manager Plus handles missing data in two ways. The first option lets the program skip over the missing values and continue plotting the next set of complete data values. If you choose the second option instead, the software makes a linear approximation of the missing data and inserts it in the graph.

Also, unlike most other graphing software, Parameter Manager Plus lets you scroll through large graphs and strip charts (charts that continue from one piece of paper to another). In fact, you can plot a graph that is 400x400 in.—slightly over 10M on a side.

If you need more than standard

Foreign exchange.
It started as a simple purchase of a box lunch on a Shibuya side street. And ended by yielding some expert travel advice from an unexpected source.
That's Tokyo. By way of United.
United can get you to Tokyo from all across this country. With friendly skies service that provides the best in international travel: fine food, fine wine, and attention to the fine details.
Because we know, like you, that the little joys along the side streets can make the fast track a lot easier.
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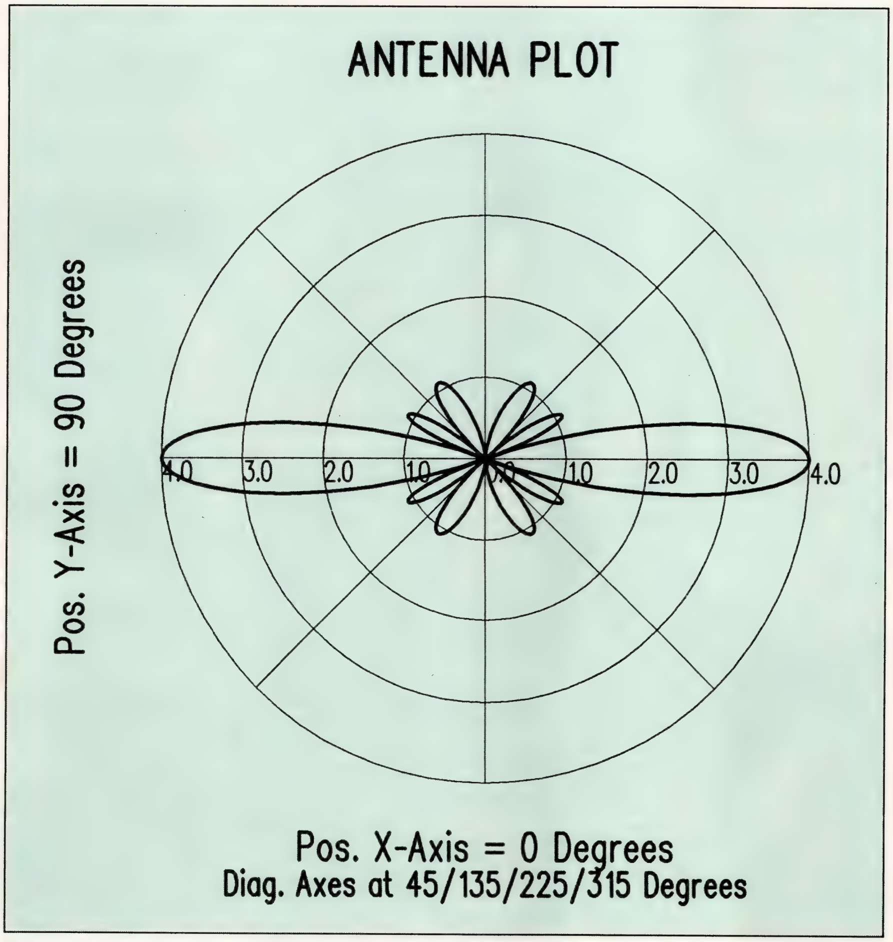



***A laserprinter produces high-quality graphs** that are ready for you to use in reports and manuals. Many graphing packages let you transfer such images directly to your word processor. (Courtesy Binary Engineering)*

x-y and log graphs, the five high-end graphing packages in **Table 1**—those costing over $200—may suit your application. In this group, you'll find packages that produce polar plots as well as surface and 3-D plots. Two packages, Tech*Graph*Pad and Templegraph, add polar plotting to the usual repertoire of x-y and logarithmic capabilities, and Surfer lets you plot 3-D surfaces. The remaining two high-end packages, Sygraph and Graftool, have both polar and 3-D capabilities.

When you investigate these five high-end packages, you move beyond the realm of the slim user's manual into the world of slip-case binders. That jump usually signifies a change from simple to complex software, too.

However, you're in for a surprise: Binary Engineering's Tech*Graph*Pad isn't complex at all. In fact, using it is almost intuitive. Kevin Shea, Binary Engineering's president, expects that most people won't read the manual—at least not at first. Even so, you should have the program running and plotting graphs in half an hour.

Tech*Graph*Pad's menus let you maneuver from setting to setting with ease; you hardly use the function keys at all. You simply select the options and functions you want and type in legends, disk-file names, and other information. If you're looking for software that can complement the suite of software tools running on your workstation, take heart. Tech*Graph*Pad runs on several types of Sun Microsystems and Digital Equipment Corporation (DEC) workstations. The workstation-based programs require an MS-DOS-emulation package.

**It's academic**

Templegraph—a program that arose from work at Temple University in Philadelphia, PA—also runs on Sun Microsystems and Hewlett-Packard workstations. Although the first sheet in the Templegraph instruction notebook says, "Don't let the size of this manual fool you...," it can be intimidating, nevertheless. Fortunately, the program incorporates a clear tree-like structure of menus that let you select options and operations by pressing the function keys on your PC's keyboard.

The only drawback to the function-key selection technique is that the keys take on new meanings as you switch from menu to menu. If you plan to plot many graphs, day after day, Templegraph can do the job. You'll need time, however, to become familiar with the menus and their actions. On the positive side, each time you select an operation, Templegraph lets you see what it does to your graph.

The two remaining graphing packages, Sygraph and Graftool, provide the widest variety of graphing features. Both packages handle standard x-y, log, 3-D, polar, and surface plots. In addition, Graftool lets you create spherical-coordinate graphs and plot complex values on a Smith chart. The program doesn't accept the values in the form 3 + i5. You must supply the complex values in pairs: a real part (3) and an imaginary part (5), which the program plots as 3 + i5.

Although the Sygraph software

seems to offer the largest variety of graphs, it requires the most documentation. The main technical manual consists of more than 900 pages. The three other manuals, which cover the command references, the program installation, and the editor, contain 250 pages in all. Sygraph is a lot like a graph-programming language. You type in command lines to open files, plot information, change legends, and perform other operations. Instead of typing in one command at a time, you can put a string of commands into a submit file that Sygraph runs in sequence to create graphs.

Besides running on IBM PCs and compatible computers, the Sygraph program runs on DEC VAX/VMS computers and on computers from Data General and NCR. You can use the program on Macintosh computers, but to do so, you must buy the Systat statistics program, which includes Sygraph and costs $595.

If you need a variety of graphs and you'd rather keep an eye on your graphs than on your programming syntax, Graftool may be for you. Like many of the other packages, Graftool uses a series of menus that let you select operations and graphing procedures. Menus appear on the left side of your display screen; the graphs take up the remaining area. Before you can get Graftool up and running, you'll need a copy of MS-DOS V3.0 or higher. The other MS-DOS-based programs covered so far can operate on V2.0 or V2.1.

### Zoom in to see new data

When running Graftool, you can conveniently zoom and pan—operations that require a bit of explanation. Panning lets you move around on a graph so you can locate points of interest that are off the display area, move them into the viewing area, and examine them. Essentially, you move a small viewing window—your display screen—across the graph. Once you have a portion of the graph in view, you can zoom in on it, magnifying it. Because Graftool stores all values to 64-bit accuracy, it can zoom by as many as 15 orders of magnitude ($1X10^{15}$).

In addition to moving around on a graph, you can view many graphs simultaneously. Obviously, there is a limit to what you'll be able to see if you try to fit 16 graphs on your display. No matter how many graphs you have on the screen, though, Graftool lets you handle as many as 4096×4096 data points in each graph. However, you'll run out of memory at about 14,400 data points.

Most of the graphing packages

## TABLE 2—ADD-IN GRAPHING-SOFTWARE PACKAGES

| COMPANY | PRODUCT | PRICE | HOST COMPUTER | LANGUAGES | COMPLEX VALUES | IMPORT FROM EXTERNAL FILES | DATA EXPORT FORMATS |
|---|---|---|---|---|---|---|---|
| CHIRP TECHNICAL SERVICES | VID & DIG (2.0) | $140 | IBM PC FAMILY | BASIC, PASCAL, C, FORTRAN | YES | NO | NONE |
| CRESCENT SOFTWARE | GRAPHPAK PROFESSIONAL (2.04) | $149 | IBM PC FAMILY | QUICK BASIC TURBO BASIC | NO | YES | PCX |
| HEARTLAND SOFTWARE | HGRAPH (4.2) | $119 | IBM PC FAMILY, VAX, SUN WORKSTATIONS | BASIC, PASCAL, C, FORTRAN, MODULA-2 | YES | NO | NONE |
| MICROCOMPATIBLES | GRAFMATIC | $135 | IBM PC FAMILY | FORTRAN (SEE TEXT) | NO | NO | NONE |
| MICROPLOT SYSTEMS | MICRO-10 (1.2) | $129 | IBM PC FAMILY | BASIC, FORTRAN, C | YES | YES | ASCII |
| NUMERICAL ALGORITHMS GROUP | PC GRAPHICS LIBRARY (MARK-2) | $595 | (SEE TEXT) | FORTRAN | YES | YES | ASCII |
| PLOTWORKS | PLOT88 (18) | $299 | IBM PC FAMILY | PASCAL, FORTAN, C | NO | YES | NONE |
| QUINN-CURTIS | SCIENCE & ENGINEERING TOOLS (6.1) | $79.95 | IBM PC FAMILY | PASCAL, C | YES | NO | NONE |
| SCIENTIFIC ENDEAVORS | GRAPHIC (4.1) | $395 | IBM PC FAMILY | C | NO | NO | NONE |

presented in **Table 1** also provide mathematical operations. The inexpensive packages let you do a few operations such as curve fitting, and the more complex and expensive programs provide for Fourier transforms, statistical functions, filtering, and other data-manipulation operations. In the future, you'll see companies integrate more and more mathematical operations into graphing-software packages. Likewise, companies that supply mathematical- and analysis-software packages will add more graphing capabilities. Eventually, it will be difficult to distinguish between the two packages.

There is already a top-down movement underway to integrate graphing software into many applications packages. Many data-acquisition software packages now include sophisticated graphing software—probably under license from one or more of the vendors listed in **Table 1**. Today, Binary Engineering is working with National Instruments (Austin, TX) to incorporate Tech*Graph*Pad in National's data-acquisition software. Because graphing is a part of the data-acquisition, -analysis, and -presentation chain, the days of stand-alone graphing-software packages may be numbered. (Very specialized graphing packages will always be available, but they'll fit into narrow markets.)

Many vendors are taking a bottom-up approach to adding graphing capabilities to software. Many companies are offering ready-made libraries and collections of add-in routines that perform primitive as well as sophisticated graphing tasks. Right now, you can add graphing routines to your Fortran, Pascal, Basic, C, and Modula-2 programs. A representative sample of nine suppliers' products appears in **Table 2.**

| GRAPHIC EXPORT FORMATS | GRAPH TYPES | GRAPH MANIPULATIONS | DATA PROCESSING | LICENSING REQUIREMENTS |
|---|---|---|---|---|
| HPGL | 2-D, 3-D, POLAR, BAR, LOG, SURFACE, SPHERICAL, SMITH, CONTOUR | AS, MS, R, Z | NO | NONE |
| PCX | 2-D, 3-D, BAR, LOG, SURFACE | AS, MS | NO | NONE |
| CGM, EPS, HPGL | 2-D, 3-D, POLAR, BAR, LOG, SURFACE, CONTOUR | MS, R | YES | NONE |
| PACKED FILE | 2-D, 3-D, BAR, LOG, SURFACE, WATERFALL | AS, MS, R | YES | PERMISSION |
| TEKTRONIX | 2-D, BAR, SURFACE, LOG | AS, MS, R | NO | NONE |
| EPS, HPGL, GKS | BAR, SURFACE, SPHERICAL, LOG, CONTOUR | AS, MS | YES | REQUIRED |
| HPGL, DMPL | 2-D, 3-D, SURFACE, LOG, CONTOUR | AS, MS | YES | PERMISSION |
| HPGL | 2-D, 3-D, BAR, LOG, CONTOUR | AS, MS, Z | YES | NONE |
| HPGL, TKF, PIC, GEM, POSTSCRIPT | 2-D, 3-D, POLAR, BAR, LOG, SURFACE, CONTOUR, SMITH | AS, MS, R, Z | YES | REQUIRED |

Unlike the stand-alone graphing-software packages that perform within a rigid set of graphing specifications, the add-in routines give you a great deal of flexibility in displaying graphical data. These routines have their own limitations, but you can combine the routines to do many things that the stand-alone packages can't. For example, if you need to place a special legend or logo on top of your graph, you'll probably find a routine that can add it for you. If such a routine doesn't exist, you may be able to combine several routines to produce the desired result.

Likewise, if you need a special data-processing routine such as a deconvolution, you can work on that algorithm and then call your add-in plotting routine to show the results. Other add-in routines add axes, legends, and tick marks. You concentrate on what you want the program to do with the data, and the prewritten graphing routines display the data for you.

Don't let the packages' graphing-routine label mislead you. Many of the packages not only draw complex and sophisticated graphs, but also offer numerical-analysis routines. Heartland's Hgraph and Microcompatibles' Grafmatic let you perform a cubic-spline fit of your data. At the other extreme, Quinn-Curtis' Science and Engineering Tools for Pascal supplies almost as many advanced mathematics routines as it does graphing routines. If you're working on a math-intensive program, the Quinn-Curtis package could save you from having to buy a math-function library.

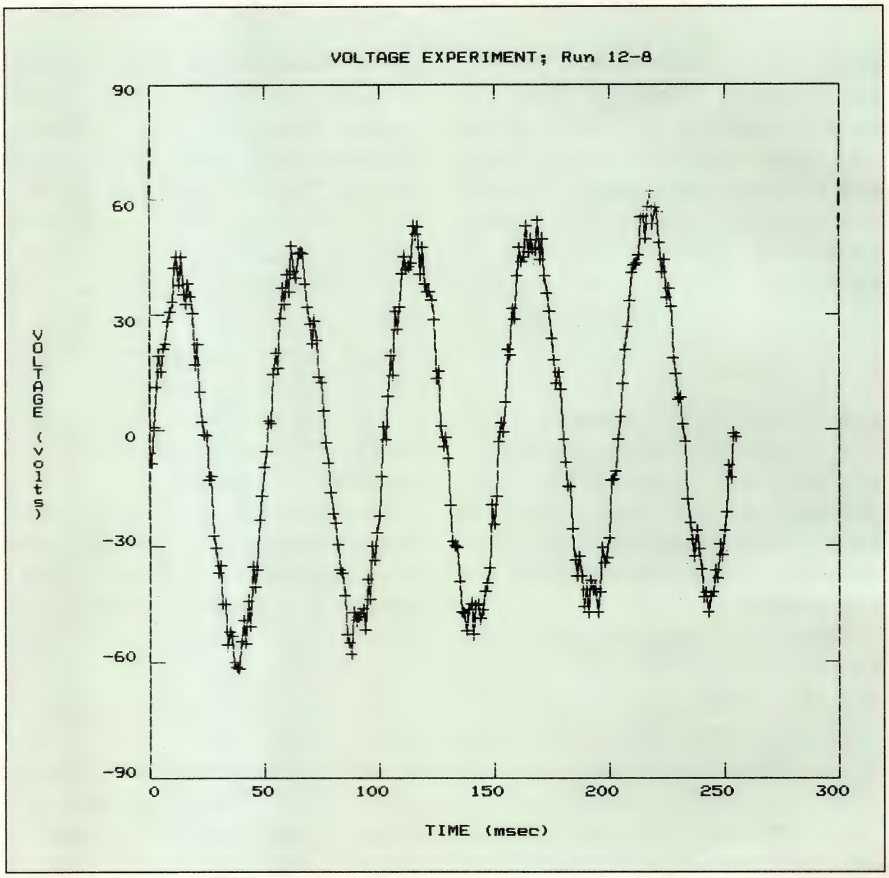
### Produce graphic files

In general, these add-in routines get data from arrays that you've set up in your program and produce the

results on a plotter or printer. Several of the programs have the ability to obtain data from bit-mapped graphics files and spreadsheet files. Some can also put the results into files for later use. All of the routines produce some form of graphic-output file that you can use to control a printer or plotter when you need a hard copy of your information.

Before you select a group of add-in routines, do your homework. Typically, you need to know if the routines do what you want them to. That statement sounds obvious, but it means that you have to know exactly what your program is supposed to accomplish. You also need to know how the routines work, how you go about using them, and what you need to get them up and running.

First, always ask for a *complete* list of the routines that are available. Some suppliers send a *representative* list of routines and several complex graphs that illustrate the power of the software. There may be no relationship between the graphs and the list of routines, so you don't know whether the supplier used one routine or 50-plus routines to draw such plots.




***A graph from a dot-matrix printer*** *is sufficient for many needs. In this example, the Graphstar software automatically scaled the axes to accommodate the data—a noisy sine wave with an increasing bias.*

Second, examine the manuals that come with the software to determine how the individual routines work. Beware of manuals that are devoid of examples and sample programs. Several manuals that accompany the routines listed in **Table 2** are good examples of what you should look for. The manual for the Microcompatibles Grafmatic library, for example, supplies details of each routine and information about the routine's restrictions. Each description also includes a realistic example of how to use the routine and a detailed explanation of the routine's effects or results. In addition, the manual contains a 50-page section of sample programs that use the routines.

The manual for Heartland's Hgraph software is also easy to follow. The manual's first part shows you how to set up the programs and how to start producing graphs. The authors use a sample Pascal program to illustrate each new concept. Don't worry if you're not a Pascal programmer; the logic in each program is clear and evident. Also, Heartland supplies routine packages for many popular languages that you can run on several different computer systems. If graphing routines are new to you, the Hgraph package might be a good place to start your education.

Microcompatibles and Heartland aren't alone in offering helpful documentation. Scientific Endeavors, Plotworks, and Quinn-Curtis also offer good materials. The Scientific Endeavors manual for the Graphic set of routines stands out because it contains an index of topics and a separate index of functions.

### Make a shopping list

After you purchase a library of graphing procedures and subroutines, you may need to purchase several other items. For example, if you're going to use the Plot88 add-in routines, a math coprocessor chip is mandatory. If your particular compiler can take advantage of a math chip, adding one to your computer can be a good investment. Scientific Endeavors reports a ninefold improvement in processing speed when a math chip handles a typical routine that makes 600 trig-function calls.

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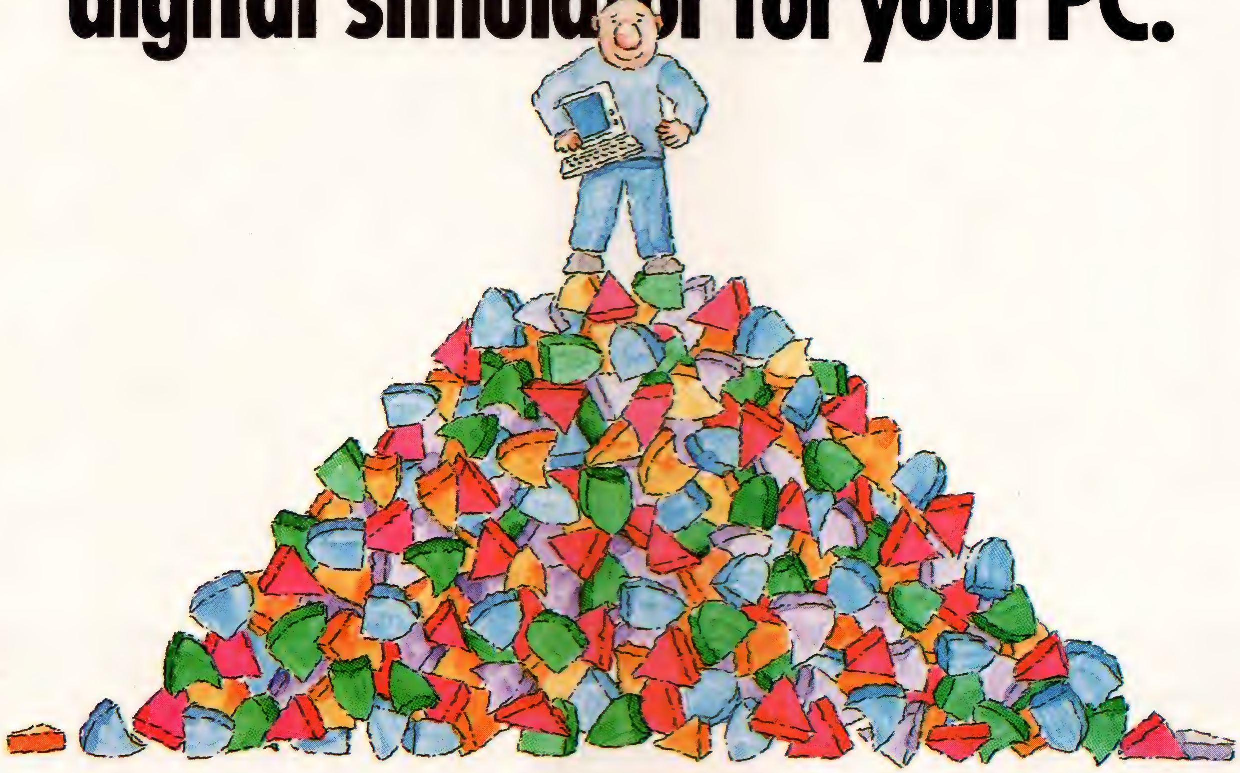

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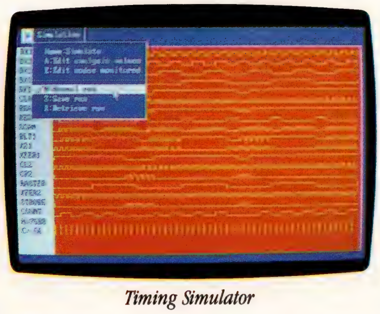

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- Multiple delay models
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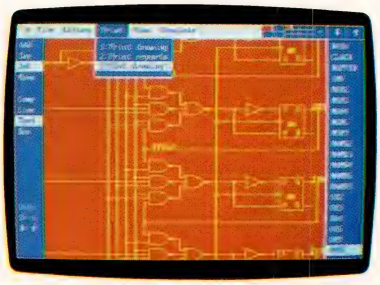

*Schematic Editor*

spectrum

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**(408) 738-4387**

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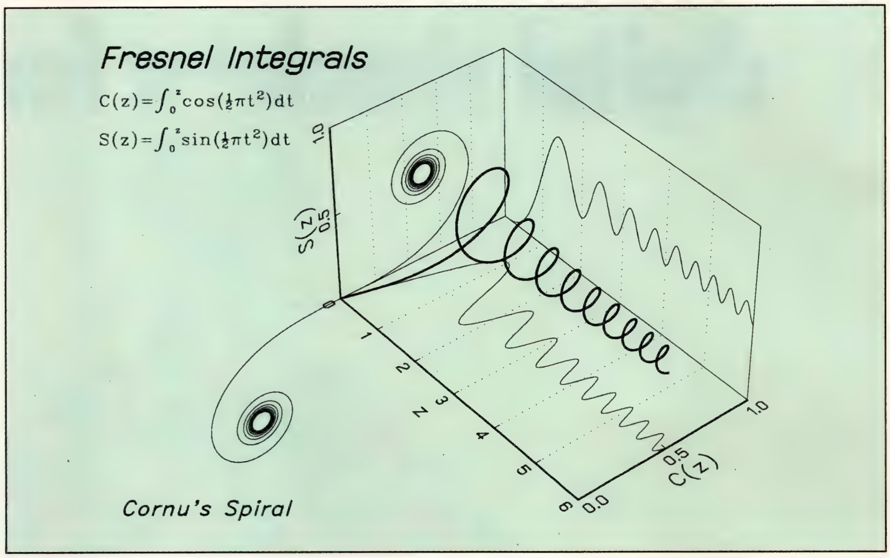
## Graphing-software packages

Of course, you need a compiler, too. Whether you use a QuickBasic, TurboPascal, or Lattice-C compiler, you can't use the routines without the basic language package you use to program your computer system. Also on the software side, if you purchase Chirp's VID & DIG library, you need Microsoft's Fortran library. Even if you program in QuickBasic, the Fortran library is a must. Chirp wrote many of its routines in Fortran, and many of those routines must link with the Fortran library's programs.

While you're making out your shopping list, you may need to add an assembler that's compatible with your host computer. If you plan to use the Graphic routines from Sci-




***Legends and formulas spruce up a graph,*** *and most of the graphing packages and routines let you position them as you like. However, not all graphing software lets you produce symbols such as the integral sign. (Courtesy Scientific Endeavors)*

## For more information . . .

To obtain more detailed information on the stand-alone and add-in graphing-software packages described in this article, contact the following manufacturers directly, circle the appropriate number on the Information Retrieval Service card, or use EDN's Express Request service.

**Binary Engineering Inc**
400 Fifth Ave
Waltham, MA 02154
(617) 290-5900
FAX 617-890-1340
**Circle No 700**

**BV Engineering**
2023 Chicago Ave, Suite B-13
Riverside, CA 92507
(714) 781-0252
TWX 650-308-9864
**Circle No 701**

**Chirp Technical Services**
Box 551
Del Mar, CA 92014
(619) 632-9510
**Circle No 702**

**Crescent Software Inc**
11 Grandview Ave
Stamford, CT 06905
(203) 846-2500
**Circle No 703**

**Edmond Software Inc**
United Founders Tower
5900 Mosteller Dr, Suite 1124
Oklahoma City, OK 73112
(405) 842-0558
**Circle No 704**

**Golden Software Inc**
Box 281
807 Fourteenth St
Golden, CO 80401
(303) 279-1021
(800) 333-1021
FAX 303-279-0909
**Circle No 705**

**Heartland Software Inc**
234 S Franklin
Ames, IA 50010
(515) 292-8216
**Circle No 706**

**Microcompatibles Inc**
301 Prelude Dr
Silver Spring, MD 20901
(301) 593-0683
**Circle No 707**

**Mihalisin Associates**
600 Honey Run Rd
Ambler, PA 19002
(215) 646-3814
**Circle No 708**

**Numerical Algorithms Group**
1101 31st St, Suite 100
Downers Grove, IL 60515
(312) 971-2337
FAX 312-971-2706
**Circle No 709**

**Plotworks Inc**
16440 Eagles Crest Rd
Ramona, CA 92065
(619) 457-5090
FAX 619-457-0946
**Circle No 710**

**Quinn-Curtis**
1191 Chestnut St, Unit 2-5
Newton, MA 02164
(617) 965-5660
FAX 617-965-7117
**Circle No 711**

**Rebus Development Corp**
2330 B Walsh Ave
Santa Clara, CA 95051
(408) 727-0110
(800) 247-4994 (CA)
(800) 654-5157
**Circle No 712**

**Scientific Endeavors Corp**
508 N Kentucky St
Kingston, TN 37763
(615) 376-4146
**Circle No 713**

**Scientific Software Solutions**
Box 956
Valley Forge, PA 19482
(215) 269-0198
**Circle No 714**

**Systat Inc**
1800 Sherman Ave
Evanston, IL 60201
(312) 864-5670
FAX 312-492-3567
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**3-D Visions Inc**
1520 23rd St
Manhattan Beach, CA 90266
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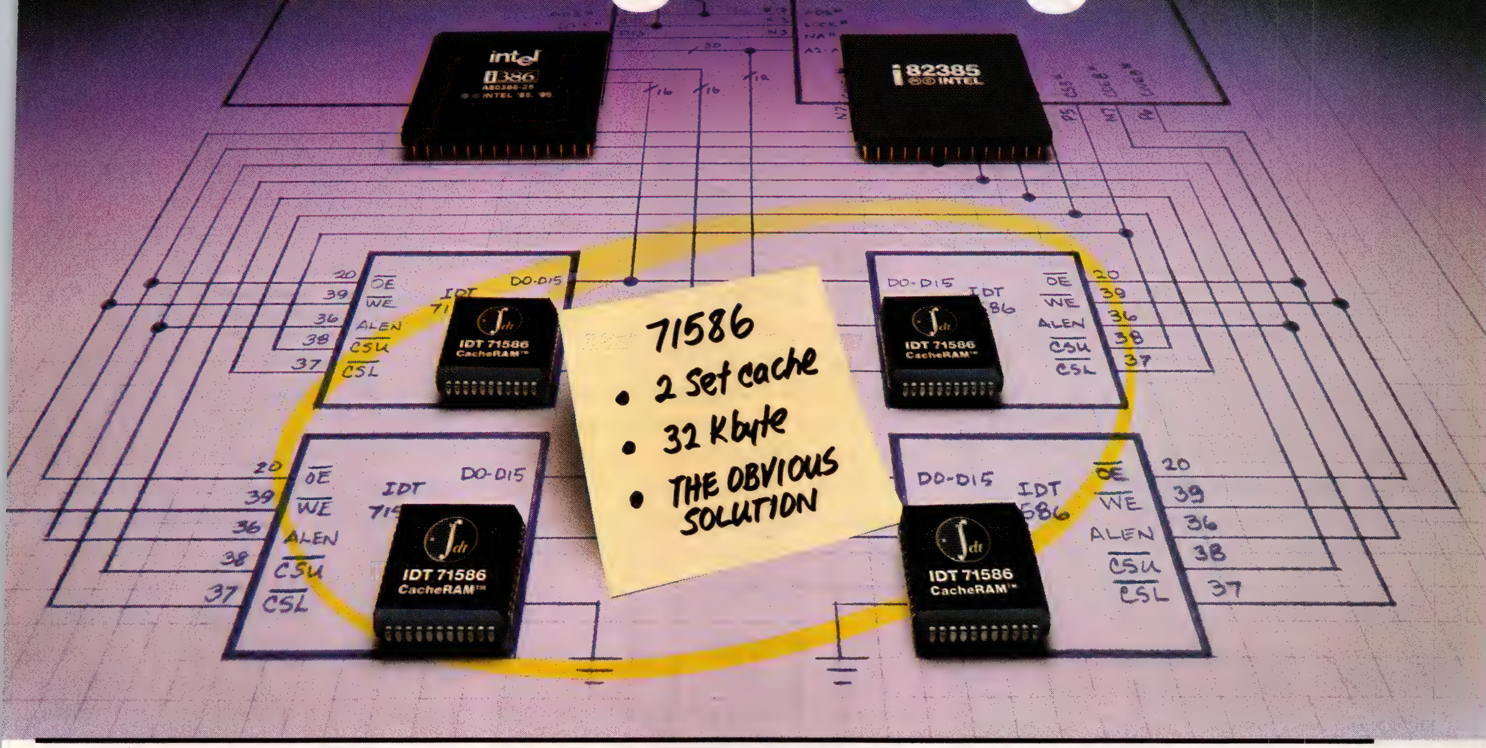


## The Intel Recommended Cache Design In 5 Chips

Now you can replace 27 ICs with only 5 chips using our new CacheRAM™, the IDT 71586. You can save two-thirds of your board space and reduce power consumption by a third. The IDT 71586 makes the ideal 2-set associative, 32K byte cache. Optimized for Intel's 82385 cache controller, the IDT 71586 matches 25MHz Intel80386™ designs with its 35ns access time.

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|---|---|
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| 20MHz | 45ns |
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| — | 25ns |

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entific Endeavors, an assembler is mandatory.

To get paper copies of the information you print on your computer's display with Graphmatic, you also need Plotmatic and Printmatic, which cost $135 each. Both libraries supply graphing and controlling software for a suite of graphics printers and plotters that operate with HPGL files. If you plan to sell a program that incorporates the graphing routines, Numerical Algorithms Group and Scientific Endeavors require licenses. Depending on your application, you may have to pay a license fee or a royalty.

### Beware of errors

While you're shopping for your software library, be sure to ask how the programs handle errors. Because you're the one doing the programming, you must pay careful attention to how the add-in routines catch and signal error conditions—if they do. Software bugs in your own software are tough enough to track down, but when they occur because of a problem in someone else's software, they can be nightmarish.

The graphing routines should come to you free of problems. However, errors can occur, particularly if you send a routine information it can't handle or understand. The routine should catch such errors that occur during run time and report them in an orderly fashion. Unfortunately, all of the graphing-routine libraries in **Table 2** give such errors only passing mention—if they mention them at all.

The Plot88 manual illustrates the problem of error detection. Although the manual provides a 3-page list of error codes and messages, you can't tell in which routines the errors occur. Even if you can locate a corresponding routine, the directions for the routine don't give a clue about where an error message or code appears.

The Graphic routines suffer from a similar problem. The manual tells you only that there are three levels of error trapping and that error messages are put in a file, GRAPHIC.ERR. It would be helpful to know what the messages are, what they mean, and where they appear in the program. It seems to be your responsibility to check the error file each time you run the program to be sure that it is free of errors.

The Quinn-Curtis routines for Turbo Pascal 4.0 and 5.0 provide some error-detecting operations. For example, the asynchronous-communication routines furnish the error codes that the manual describes. However, you have to look through the manual procedure by procedure to determine which routines supply any error-detecting steps. Few of the add-in routines in any of the libraries we examined do any internal error checking.

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**The Casio fx-7000G $89.95.** It's the world's first programmable scientific calculator with a graphic display. It can give form to your figures, instantly drawing graphs that depict your formulas and calculations.

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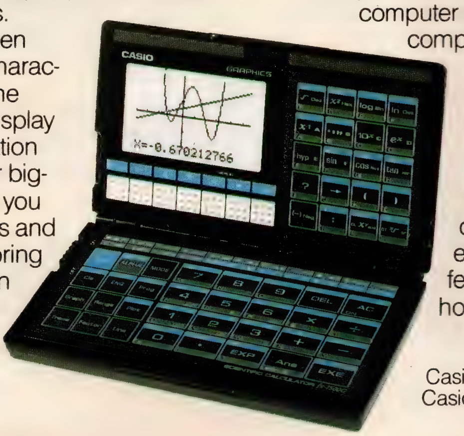

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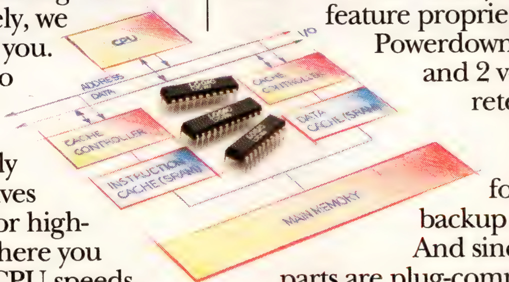


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| 16K x 4 | SEP I/O TRANSP/WRITE | 20 |
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## DUAL-PORT STATIC RAMs

# Specialized memories ease communications

The popularity of dual-port static RAMs is on the rise. These devices greatly simplify shared-memory implementations.

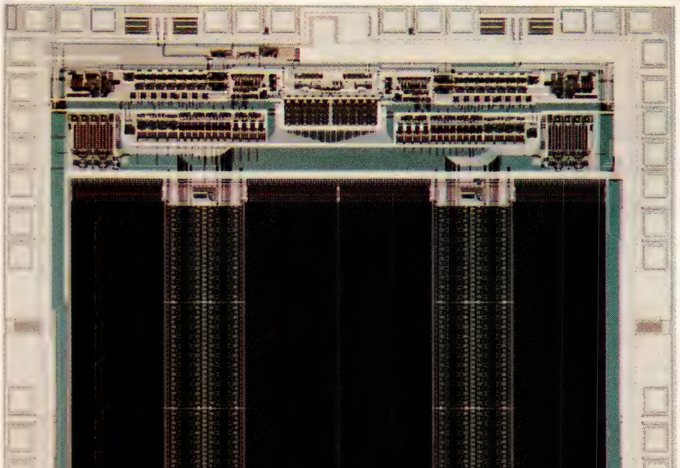
**Dave Pryce,**
*Associate Editor*

Although they make up only a small fraction of the hundreds of millions of RAMs produced each year, dual-port static RAMs (SRAMs) are becoming increasingly important for solving difficult interface problems. Compared with the ubiquitous single-port dynamic RAMs (DRAMs) used in conventional memory applications and the dual-port dynamic RAMs (VRAMs) used in video graphics applications, dual-port static RAMs are less familiar to designers. They're a valuable addition to your computer-equipment design arsenal, however, because they provide a simple way to untangle such snags as arbitration problems in shared-memory systems.

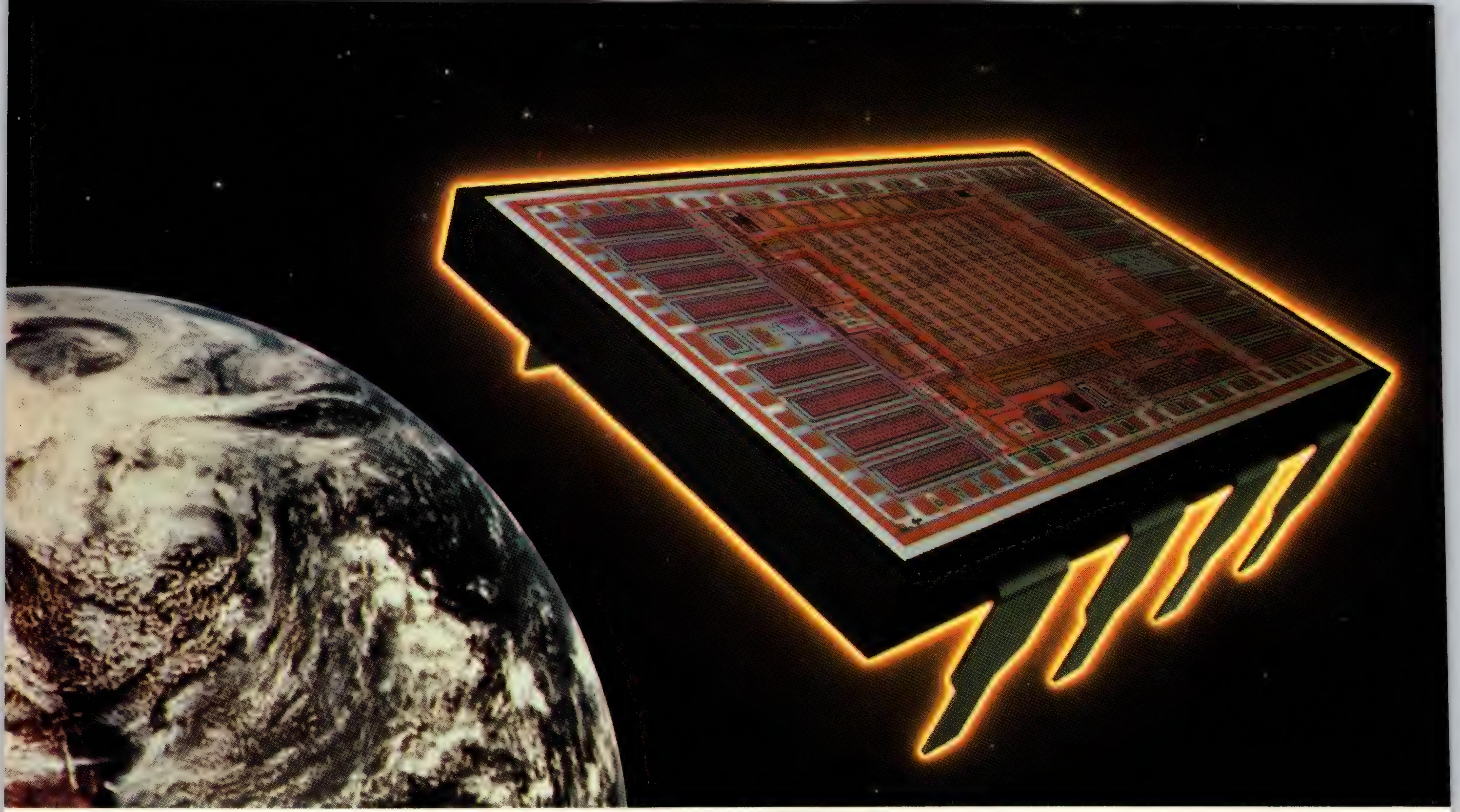
Unlike dual-port dynamic RAMs (VRAMs), which are serial on one side and parallel on the other, dual-port SRAMs have parallel ports on both sides. These parallel ports let you use dual-port SRAMs for local memory that is shared between two systems, such as two CPUs, or for communications and real-time DSP applications that require asynchronous communication between two devices at the same time.

Fig 1 illustrates a typical application in which three dual-port SRAMs interface a host CPU to another CPU, a DSP, and an I/O controller. Because of the unique capabilities of dual-port chips, you can use the same memory for both working storage and communication between two devices, thus avoiding the need for special data-communication hardware.

Dual-port SRAMs provide a faster and less complex alternative to conventional single-port RAMs, which have inherent speed limitations because of their



***This 2k × 8-bit dual-port static-RAM chip*** *from Cypress Semiconductor is available in a 48-pin plastic DIP, ceramic DIP, or leadless chip carrier (LCC).*



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CIRCLE NO 107

## Dual-port static RAMs

need for multiplexed read/write (R/W) access. Dual-port SRAMs allow two independent devices to have simultaneous R/W access to the same memory. The devices communicate with each other by passing data through the common memory.

Although the market for dual-port SRAMs is growing at a rate of over 30% a year, its total dollar value is small. The market for these chips is estimated to be only $15 million in 1989 and $20 million in 1990. Consequently, only a handful of vendors currently serve this niche market. Integrated Device Technology (IDT) is probably the leading supplier, with at least eight different products. Other major players include Cypress Semiconductor, Fujitsu Microelectronics, Sharp Microelectronics, Vitelic Corp, and VLSI Technology.

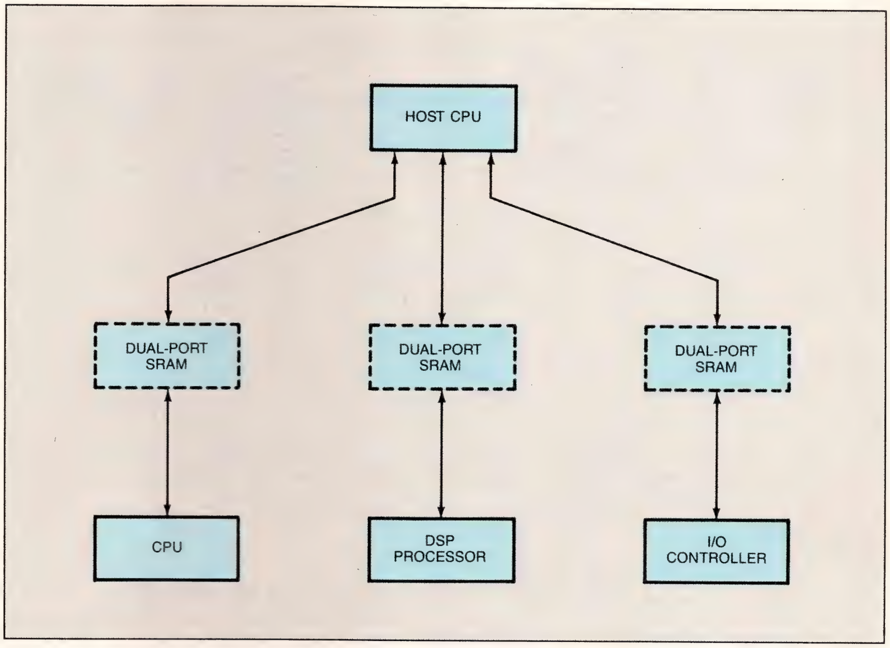


***Fig 1—Because dual-port SRAMs provide a shared memory,*** *you can use them as a communications interface between a host CPU and other processors and controllers.*

Dual-port SRAMs are available in speed ratings from 35 to 120 nsec. At least one supplier (Cypress Semiconductor) expects to announce 25-nsec versions by mid-year. The densities of currently available chips range from 8k to 128k bits. Chip organizations range from 1k × 8 to 16k × 8 bits and 2k × 16 to 8k × 16 bits. By mid-1989, Integrated Device Technology expects to introduce 1k × 8-bit and 2k × 8-bit 4-port SRAMs, which are even more versatile than their dual-port siblings.

In a unique departure from the typical architecture, VLSI Technology has created a dual-port SRAM that is organized as 1k × 16 *and* 2k × 8 bits. According to VLSI Technology, its VT16DP8 chip is the industry's first single-chip solution to the problem of transferring data between systems having dissimilar word sizes. The chip allows simultaneous reads and/or writes from either the 16-bit or the 8-bit port. The 16-bit port has the ability to read or write in either word or byte mode.

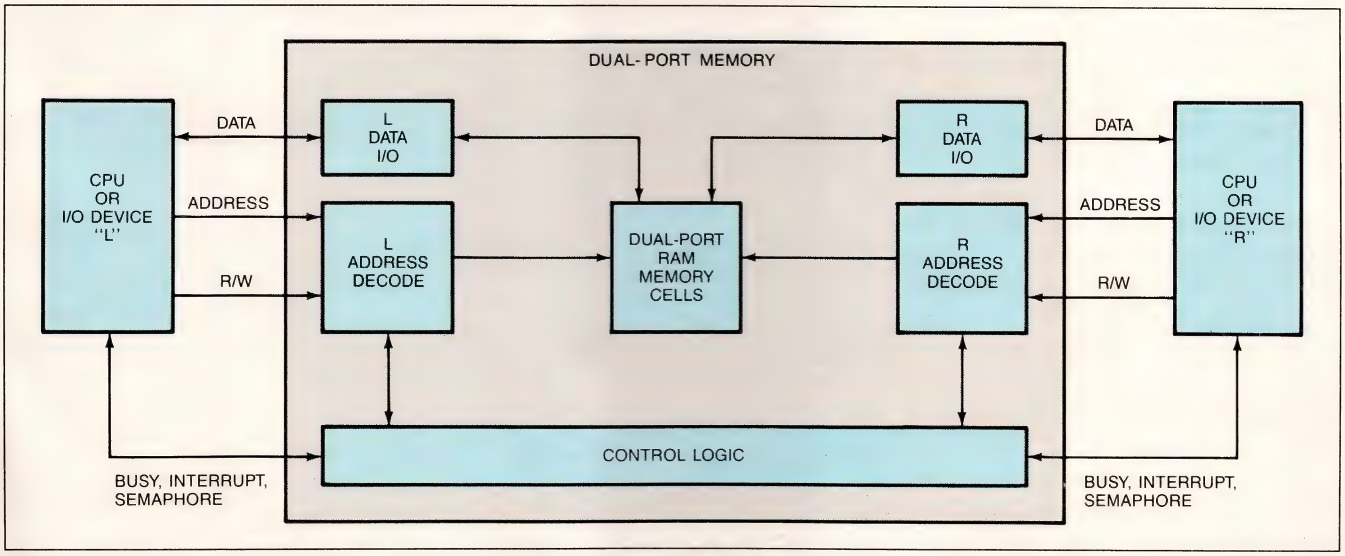


***Fig 2—Typical of a dual-port SRAM's architecture,*** *this block diagram of a chip from Integrated Device Technology shows two sets of address, data, and read/write control signals, each of which accesses the same set of memory cells.*

## Dual-port static RAMs

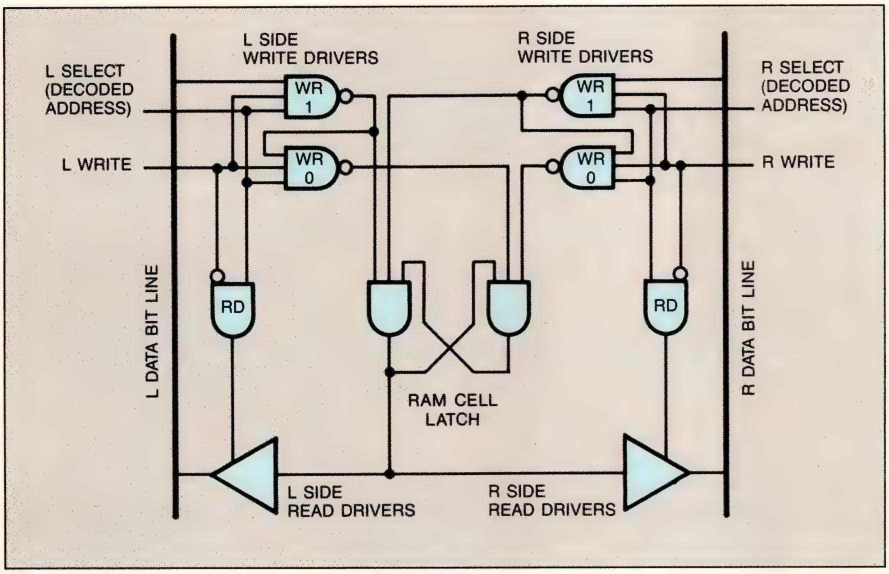


***Fig 3—Both the L and the R select lines of this dual-port RAM cell*** *can independently and simultaneously select the cell for readout. Moreover, either side can write data into the cell. Arbitration logic resolves any conflict that occurs when both sides try to write data to the same cell at the same time.*

As you would expect, prices for dual-port SRAMs vary widely, depending on density, speed, packaging, and grade (commercial or military). Some typical prices (in quantities of 100) for commercial-grade parts in the fastest available speed rating (usually 35 nsec) are: 1k×8 bits, $28; 2k×8 bits, $46; 4k×8 bits, $60; and 2k×16 bits, $103.

The previously mentioned VT16DP8 from VLSI Technology is a 70-nsec device that sells for $52.50 (1000). At the low end of the price range, Fujitsu has a relatively slow (90-nsec) 2k×8-bit device that sells for $12 (1000).

The basic architecture of a dual-port SRAM includes two sets of address, data, and control lines (**Fig 2**). Each set of lines (left and right) can independently and simultaneously access any word in the memory, even when both sides are accessing the same memory location at the same time.

Built-in arbitration (in the form of interrupt logic and busy logic) resolves any conflict in memory access when both the left and the right sides try to read or write to the same memory location simultaneously. Some dual-port chips include semaphore logic, which aids in software-oriented arbitration.

The memory cell for a dual-port SRAM is a true dual-access cell. This cell has two independent and separate address-select lines and data-bit lines that have access to the RAM cell latch (**Fig 3**). The L and R select lines can independently and simultaneously select the cell for readout. Moreover, either side can write data into the cell. Arbitration logic (not shown in **Fig 3**) resolves any conflict that occurs when both sides try to write data into the cell at the same time.

### Arbitration logic is the key

As mentioned, dual-port SRAMs use one or more types of arbitration logic—interrupt, busy, and semaphore logic—to resolve conflicts. Some chips provide all three forms of logic.

Interrupt logic provides signaling between two processors that share a common memory. A common form of signaling is for one processor to cause an interrupt on the other processor. In this way, the receiving processor is informed of a communication without having to check for it continually.

Busy logic resolves any conflict that occurs when both ports of the dual-port chip attempt to access the

**TABLE 1—REPRESENTATIVE DUAL-PORT SRAMs**

| MANUFACTURER | SIZE (BITS) | ARBITRATION LOGIC: INTERRUPT | BUSY | SEMAPHORE | SPEED RANGE (NSEC) |
|---|---|---|---|---|---|
| CYPRESS SEMICONDUCTOR | 1k×8 | ● | ● | | 35 TO 55 |
| | 2k×8 | ● | ● | | 35 TO 55 |
| INTEGRATED DEVICE TECHNOLOGY | 1×8 | ● | ● | | 35 TO 100 |
| | 2k×8 | ● | ● | ● | 35 TO 100 |
| | 4k×8 | | | ● | 35 TO 70 |
| | 8k×8 | ● | ● | ● | 35 TO 70 |
| | 16k×8 | ● | ● | ● | 35 TO 70 |
| | 2k×16 | | ● | | 45 TO 90 |
| | 4k×16 | ● | ● | ● | 30 TO 70 |
| | 8k×16 | ● | ● | ● | 30 TO 70 |
| FUJITSU MICROELECTRONICS | 2k×8 | ● | ● | | 90 TO 120 |
| SHARP MICROELECTRONICS | 2k×8 | ● | ● | | 35 TO 55 |
| | 4k×8 | ● | ● | | 35 TO 55 |
| VITELIC CORP | 2k×8 | | ● | | 55 TO 90 |
| VLSI TECHNOLOGY | 2k×8 AND 1k×16 | ● | ● | | 70 |
| | 2k×8 | ● | ● | | 30 TO 45 |

same address at the same time. Such a situation can arise when one port is trying to read the same data that the other port is writing, or when both ports attempt to write to the same word at the same time.

Semaphore logic provides a set of token-passing flags that supports the block allocation of memory. Although block allocation of memory is a software technique, it can benefit from this hardware support. The semaphore logic connects to external pins, and the internal flags indicate which CPU has permission to use a block of memory.

Many applications for dual-port SRAMs require greater memory depth and/or width than a single chip can provide. In these cases, using two or more chips is the only answer.

You can expand the depth of dual-port SRAMs with little trouble. For example, four 2k×8-bit chips make an 8k×8-bit memory. You can also expand the width of dual-port SRAMs, but you must be careful how you do it. Although, for example, two 2k×8-bit chips make a 2k×16-bit memory, you can't simply connect the chips to each other.

Because several hardware arbitrators are active at the same time, expanding the memory width can create a problem. Although you can provide selective arbitration by adding external logic to the chip-enable pins of additional dual-port chips, a better solution is to use master/slave chips in combination.

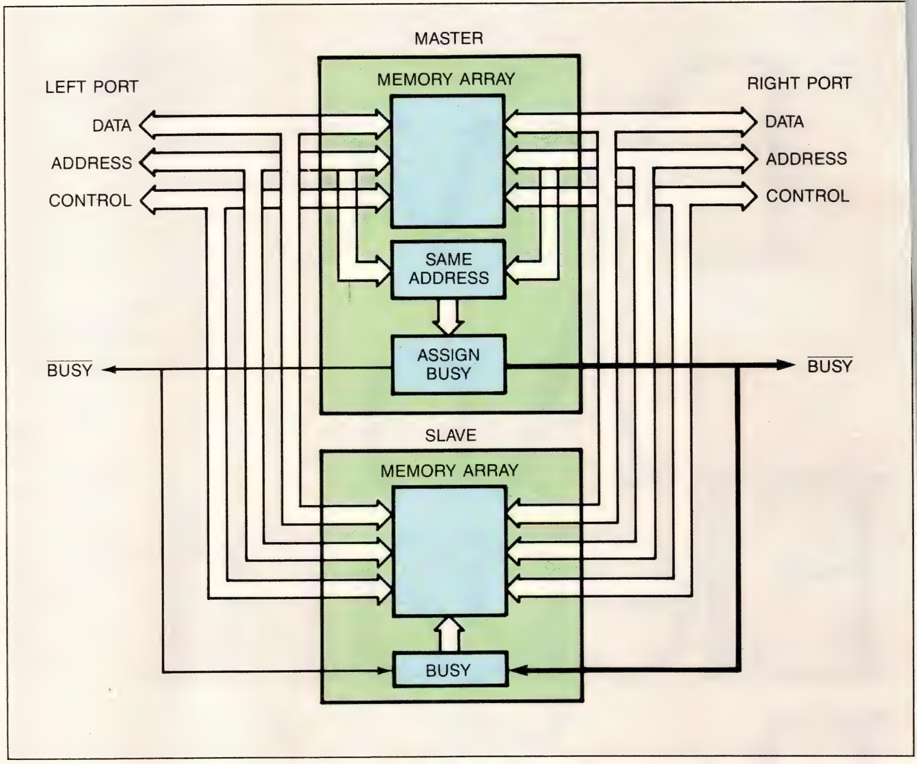


***Fig 4—One solution to the system-deadlock problem*** *that occurs when you expand dual-port SRAMs in width is to use master/slave chip combinations. If the master chip activates the Busy function, the slave chip internally disables the write signal of the losing side, thus making only one side accessible.*

In master/slave combinations, the master chip has complete control over the slave chip and decides which side has complete access to a particular memory location at a given time (**Fig 4**). Unlike a master dual-port chip, a slave chip uses its Busy pin as an input rather than an output. Thus, if the master chip activates the Busy function, the slave chip internally disables the write signal of the losing side, making only one side accessible.

When expanding dual-port SRAMs in width, you must make the slave chips wait to write until after the Busy input at the slave has settled. Otherwise, the slave chips may begin writing while the busy signal is settling. This condition is true for systems using conventional dual-port chips with external slave logic as well as for sys-

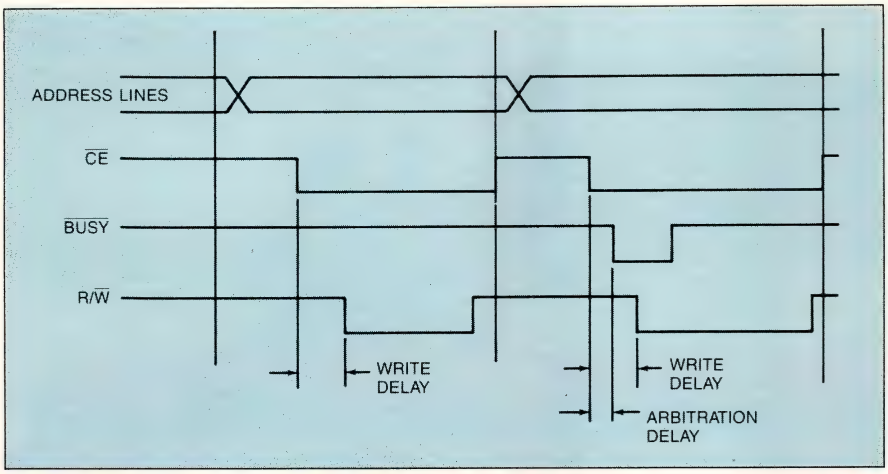


***Fig 5—When expanding dual-port SRAMs in width,*** *you must make the slave chip wait to write until after the busy input at the slave has settled. This write delay is required only in width-expanded systems that use slave chips, not in single-chip or depth-expanded systems where only one chip is active at a time.*

tems using slave chips.

**Fig 5** shows how to accomplish the needed delay in the slave chip's writing: You delay the write enable to the slave by the arbitration time of the master chip. This write delay is only needed in width-expanded systems that use slave chips, not in single-chip systems or depth-expanded systems where only one chip is active at a time.

For a clear and detailed explanation of SRAM timing requirements, as well as arbitration schemes, expansion methods, and other information on the workings of SRAMs, you can consult two excellent application notes from IDT (**Refs 1** and **2**). Much of the technical content of this overview of dual-port SRAMs is based on information contained in these notes. Complete technical information on SRAMs is somewhat scarce because of the relatively small number of SRAM manufacturers, so these two notes are especially valuable sources of information.

The availability of true dual-port memory chips lets you implement high-speed communication between components of computer-based systems while avoiding many of the problems associated with earlier systems that provide direct memory access.

Because of the speed and versatility of dual-port SRAMs, you can expect these chips to appear as standard components in a variety of applications, from computers, disk controllers, and modems to copiers, printers, and mobile telephones. EDN

## References

1. Miller, Michael J, *Dual-Port RAMs With Semaphore Arbitration*, Application Note AN-14, Integrated Device Technology Inc, Santa Clara, CA, 1987.
2. Wyland, David C, *Dual-Port RAMs Simplify Communication in Computer Systems*, Application Note AN-02, Integrated Device Technology Inc, Santa Clara, CA, 1987.

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## For more information . . .

For more information on the dual-port SRAMs discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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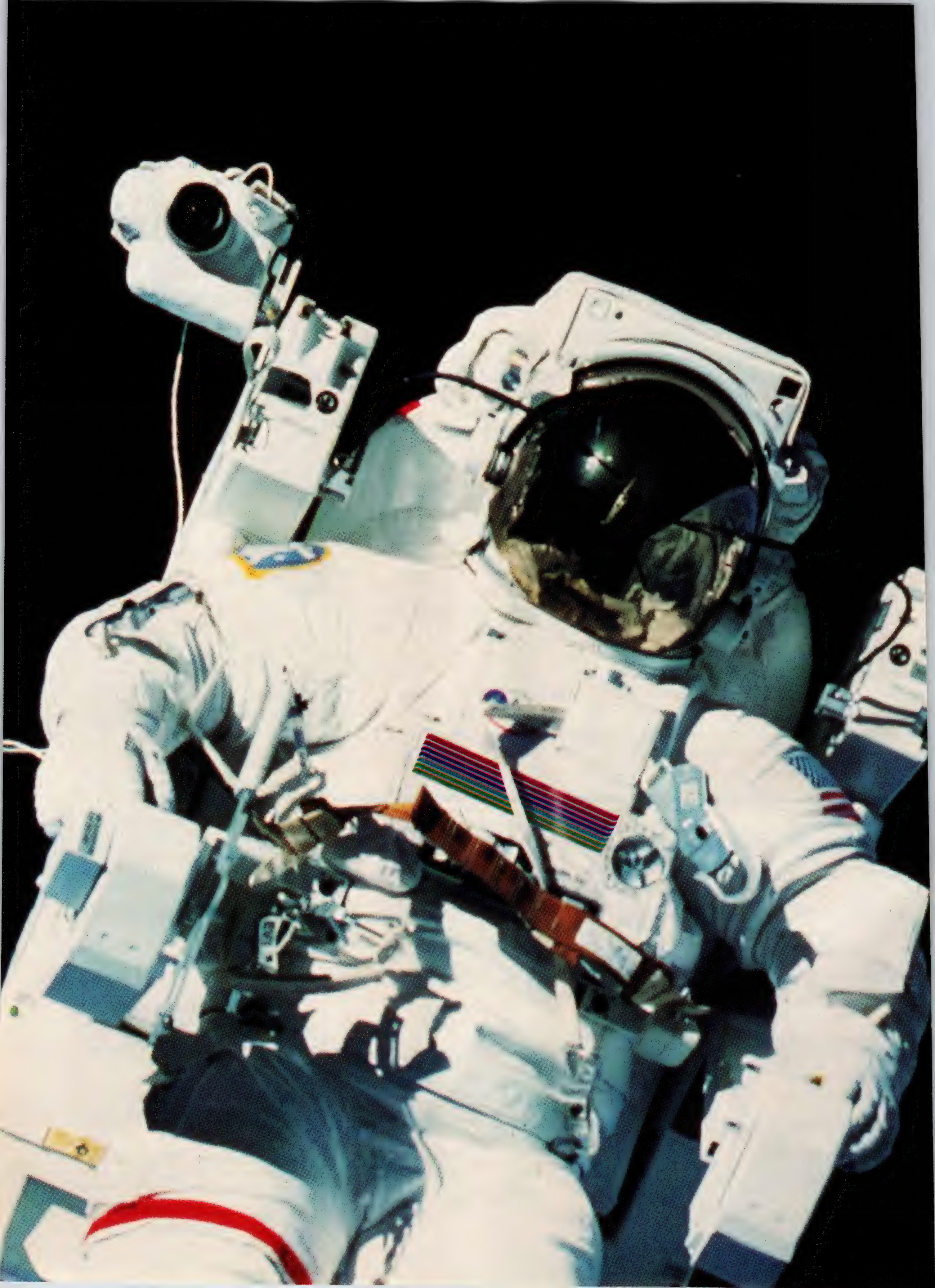

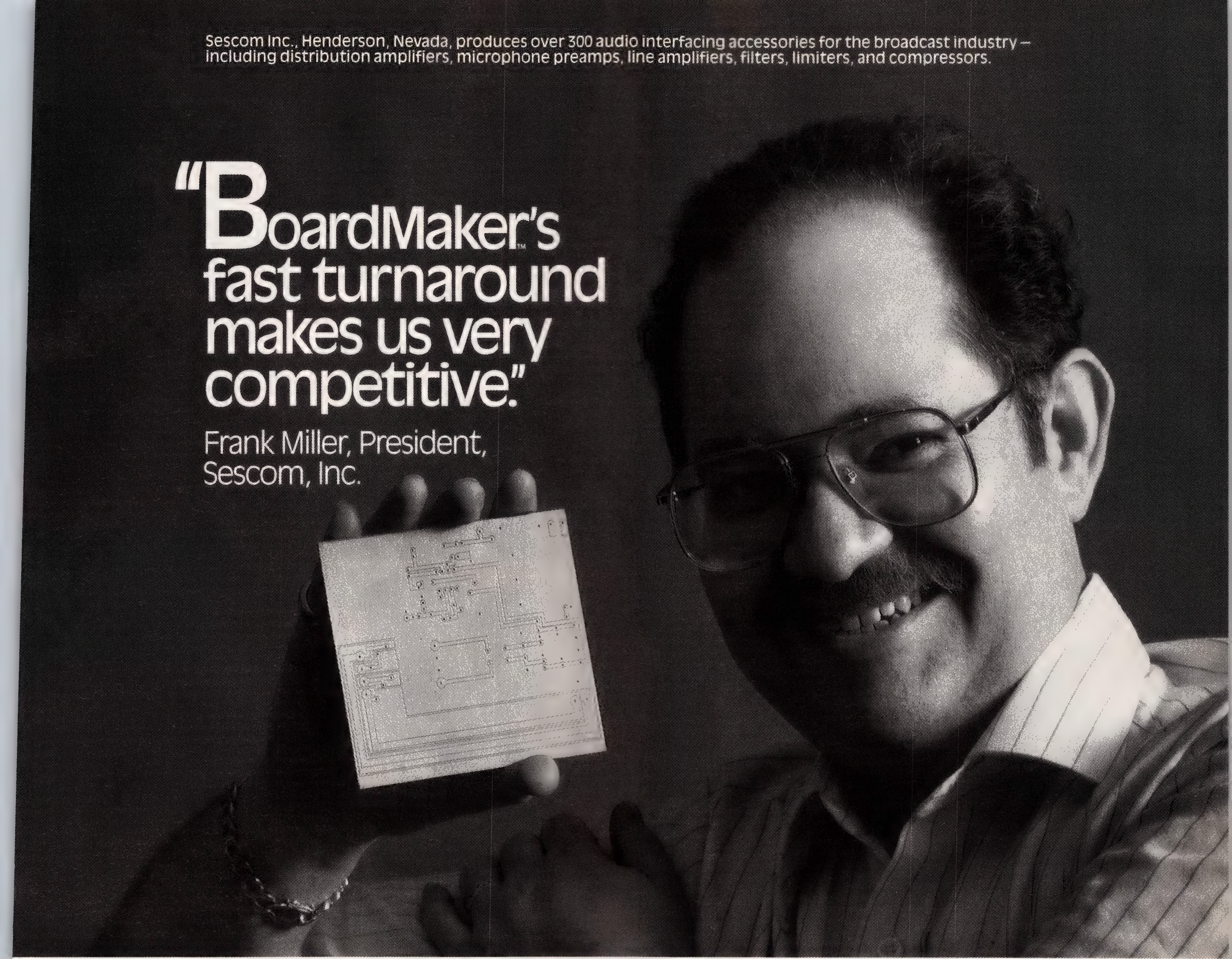


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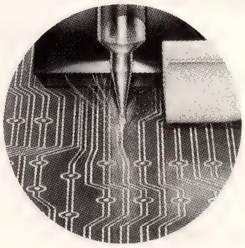

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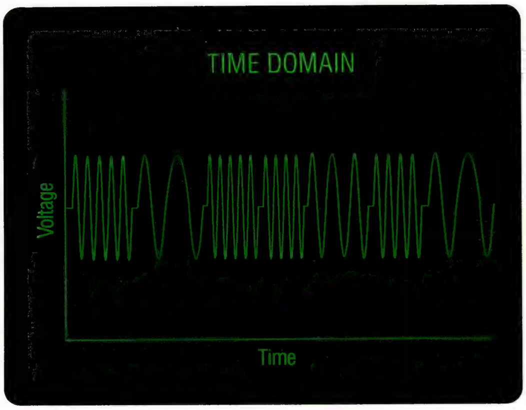
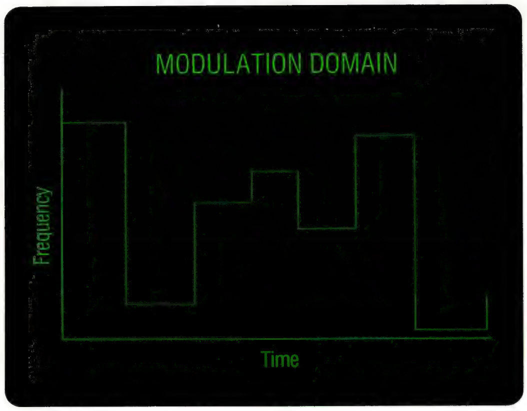
hop, hop, hop,

chirp, chirp,

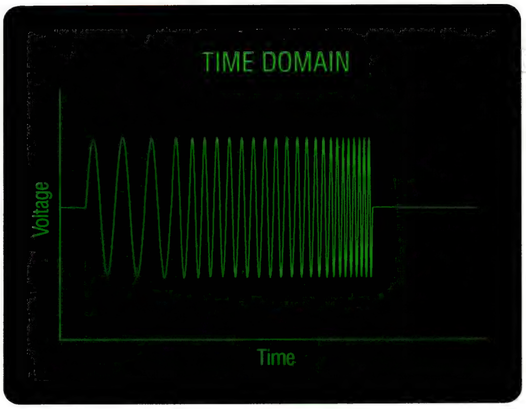
jitter, jitter,

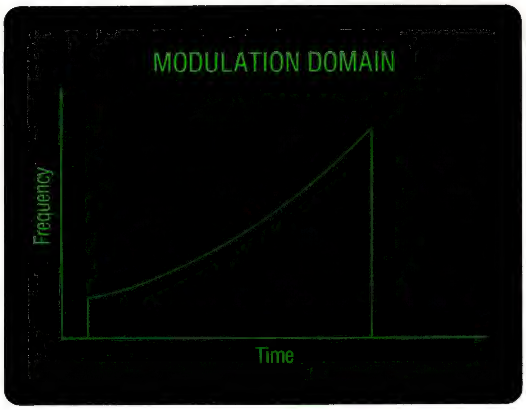
# ...like you've never seen them before.



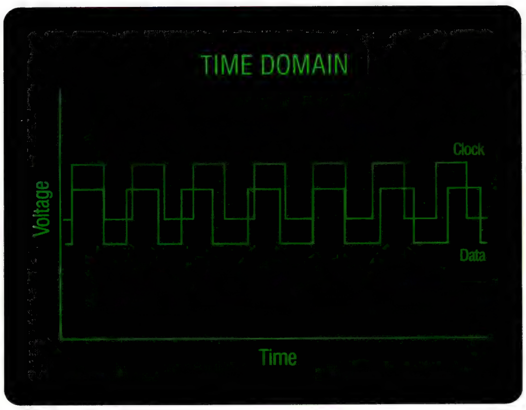



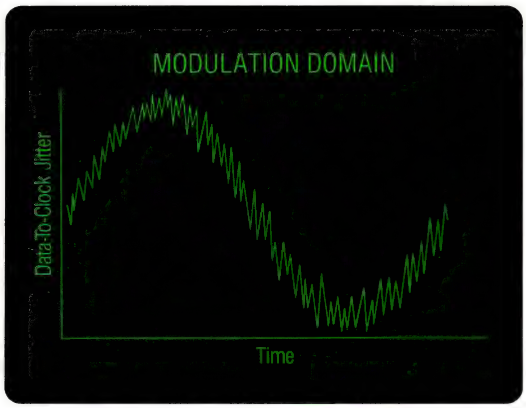

*hop* *...a time-domain view of a frequency-agile signal (left) reveals little useful information. The new modulation-domain view on the right clearly shows the hopping sequence, settling times, and channel frequencies.*



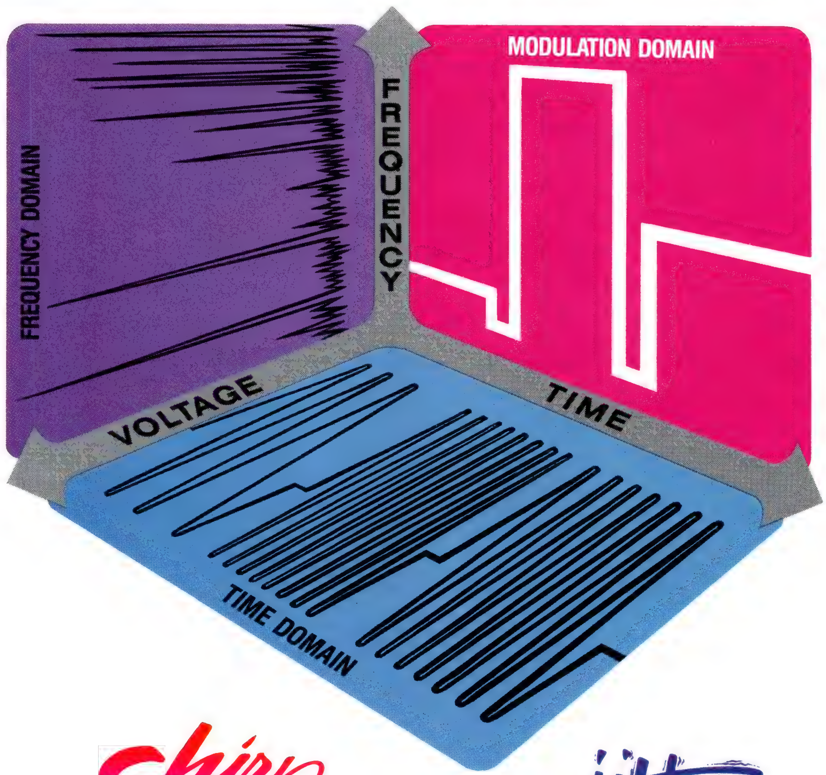

*chirp* *...no quantitative data is available from the time-domain view of a radar chirp on the left. However, the frequency vs time display of this single-shot event clearly shows chirp linearity and frequency.*




*jitter* *...a time-domain view of jitter shows only that the jittered data's edge is constantly changing with respect to the clock. In the modulation domain, the jitter magnitude and periodic content are clear.*

# HP introduces the modulation domain.

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Like its predecessors — scopes and spectrum analyzers — the frequency and time interval analyzer is sure to give designers greater insight into system problems, and provide dramatic savings in product development and manufacturing. That's the best reason yet to explore the modulation domain. So contact your local HP sales office for additional product information on the HP 5371A. Now, it's up to you.

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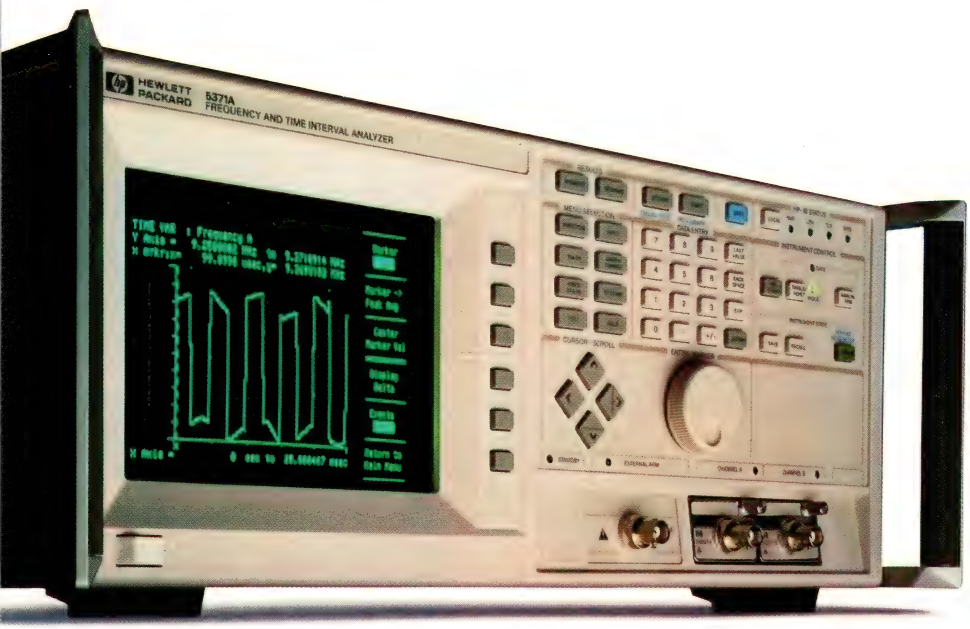
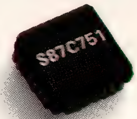



# Macro performance in a micro size

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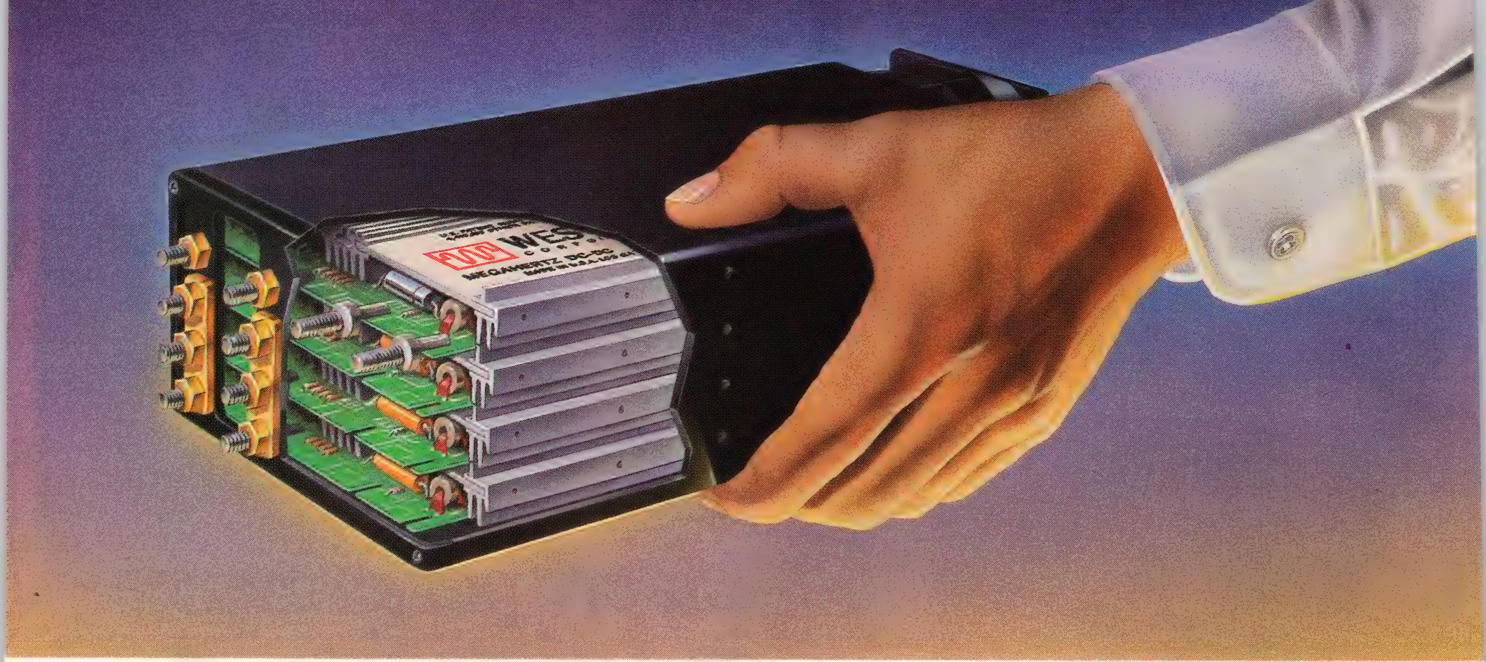
# THE POWER SUPPLY



# REDEFINED

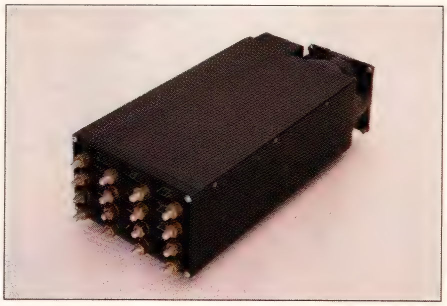
**THE WESTCOR STAKPAK™. NEW GENERATION 250 TO 1200 WATT SINGLE OR MULTIPLE OUTPUT OFF-LINE SWITCHER. 3.2 X 5.5 X 11.4 INCH CASE. FAN-COOLED.**

Stack the odds in your favor by designing-in Westcor's 6 watt/cubic inch high power megahertz switcher. Capitalizing on patented and proven megahertz module technology and innovative thermal management techniques, the StakPak provides up to 1200 watts of power at 50°C with 1 to 8 isolated and fully regulated outputs.

For existing designs the StakPak's small size and low profile allow system enhancement without mechanical redesign. Simply replace your open frame switcher with up to 1200 watts of StakPak power or replace your "box switcher" with 2 StakPaks and realize up to twice the power without losing additional space. StakPak power factor correction provides 850 watts of output power from a standard 115 VAC wall outlet. In new designs, more space can be devoted to functionality or the system can be downsized.

The StakPak's 8 module output section can be factory configured in virtually an infinite number of voltage, current and power combinations. Special models providing between 250 to 1200 watts and outputs from 2 to 95 VDC are available.

Other features include outstanding electrical performance; UL, CSA, VDE safety agency approval (in process); variable speed fan option for low ambient noise enviroments and 3 phase or DC input options. Indeed, with unprecedented power density, versatility and new features, the StakPak redefines power packaging. Please contact Westcor for a data sheet, pricing and additional information.



STANDARD 1200 WATT STAKPAK MODELS (110/220 VAC input)

| Model | Output Voltage (VDC) and Maximum Current (amperes) per Channel #1 | #2 | #3 | #4 | #5 |
|---|---|---|---|---|---|
| Single Output | | | | | |
| SP1-1801 | 2 @ 240 | | | | |
| SP1-1802 | 5 @ 240 | | | | |
| SP1-1803 | 12 @ 100 | | | | |
| SP1-1804 | 15 @ 80 | | | | |
| SP1-1805 | 24 @ 50 | | | | |
| SP1-1806 | 28 @ 42 | | | | |
| SP1-1807 | 48 @ 25 | | | | |
| Dual Output | | | | | |
| SP2-1801 | 2 @ 120 | 5 @ 120 | | | |
| SP2-1802 | 5 @ 120 | 5 @ 120 | | | |
| SP2-1803 | 5 @ 120 | 12 @ 66 | | | |
| SP2-1804 | 12 @ 66 | 12 @ 66 | | | |
| SP2-1805 | 15 @ 53 | 15 @ 53 | | | |
| Triple Output | | | | | |
| SP3-1801 | 5 @ 180 | 12 @ 16 | 12 @ 16 | | |
| SP3-1802 | 5 @ 150 | 12 @ 33 | 12 @ 16 | | |
| SP3-1803 | 5 @ 180 | 15 @ 13 | 15 @ 13 | | |
| SP3-1804 | 5 @ 150 | 15 @ 26 | 15 @ 13 | | |
| Quad Output | | | | | |
| SP4-1801 | 5 @ 150 | 12 @ 16 | 12 @ 16 | 5 @ 30 | |
| SP4-1802 | 5 @ 150 | 15 @ 13 | 15 @ 13 | 5 @ 30 | |
| SP4-1803 | 5 @ 150 | 12 @ 16 | 12 @ 16 | 24 @ 8 | |
| SP4-1804 | 5 @ 150 | 15 @ 13 | 15 @ 13 | 24 @ 8 | |
| Five Output | | | | | |
| SP5-1801 | 5 @ 120 | 12 @ 16 | 12 @ 16 | 5 @ 30 | 24 @ 8 |
| SP5-1802 | 5 @ 120 | 15 @ 13 | 15 @ 13 | 5 @ 30 | 24 @ 8 |

Total output power may not exceed 1200 watts for any model, single or multiple output. Lower power StakPak models are available. Please contact the factory.

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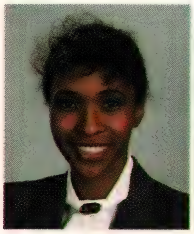
# Design choices let you optimize Nubus access



You can design a reliable Nubus interface as long as you observe good design practices and keep some caveats in mind.

*J D Mosley,*
*Regional Editor*

To take full advantage of the Nubus's features—which include a 32-bit backplane with multiprocessing capability, multiplexed address and data lines, and a 10-MHz clock—you can either design your own boards, adapt existing boards to the Nubus backplane, or purchase one of the many Nubus-compatible boards currently available. If you choose to modify existing boards or design new boards and integrate them into a Nubus system such as the Macintosh II, you must adhere to specific design practices. You can detour the pitfalls of interface design by heeding some specific tips from the design veterans of the Nu-Group—the Nubus Manufacturers and Users Group. By avoiding any tempting design shortcuts, you'll supply end users with a Nubus interface that is free of potential problems and, ultimately, extend your system's life in the market.

The major attraction of the Nubus design is its simplicity: It can identify expansion boards (also called modules) as soon as they are plugged into the bus. End users don't need to set DIP switches or use jumpers when adding boards or reconfiguring the computer system.

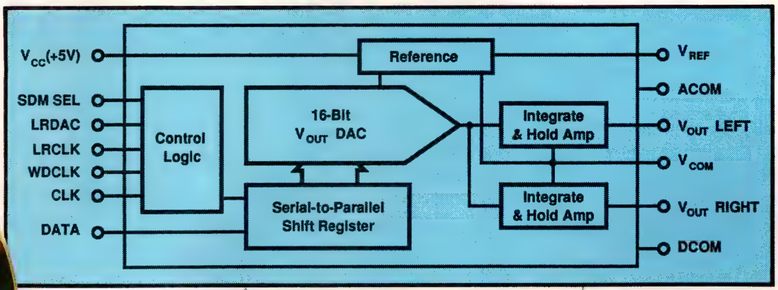
The Nubus uses a geographical addressing scheme to identify boards connected to the bus and provide automatic system configuration. Each of the 16 available slots in the Nubus backplane has a unique identity and a specific 16M-byte address space, which is referred to as a *slot space.*

The board determines its slot location by sampling the four bus signals that provide the code. A configuration ROM located on each board lets the computer's initialization software dynamically detect each board's resources when you power up your system.

According to the preliminary IEEE-1196 specification, the Nubus's fair-arbitration technique ensures that all

***Many manufacturers now offer Nubus computers.*** *The Explorer II, for example, is a Texas Instruments Nubus-based machine that uses triple-size (11.024 × 14.437-in.²) Nubus expansion boards rather than the PC-size (4.0 × 12.875-in.²) boards used in the Macintosh II.*

# The Portable Digital Audio DAC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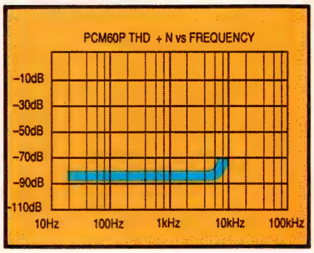


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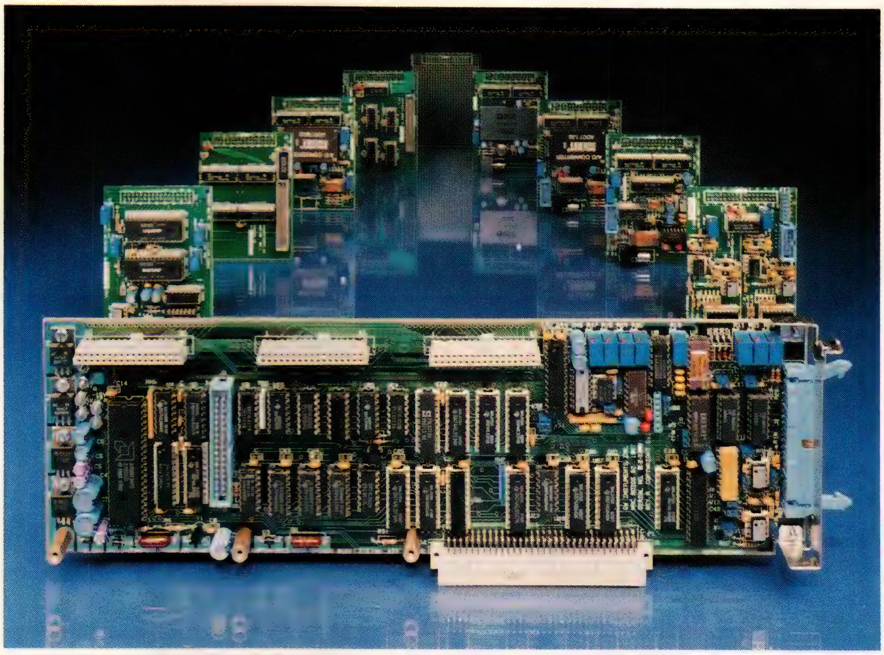
## Nubus interface options

boards have equal access to the bus. The Nubus uses an algorithm to eliminate the possibility that a low-priority board might never obtain access to the bus. According to the fair-arbitration scheme, boards plugged into slots with high identification numbers are given priority in the arbitration contest. The bus uses four dedicated arbitration lines and distributed arbitration logic. Two cycles after the start of an arbitration contest between boards, the arbitration lines transfer access to the next bus owner. In contrast to the priority-ranking arbitration scheme used in the Micro Channel, this equal-access scheme can't be overridden.

In addition to noting the Nubus's simplicity, the P-1196 specification states that the Nubus is optimized for 32-bit transfers and multiprocessor operation. The bus can address as much as 4G bytes of memory and can perform 32-bit data transfers at 20M bytes/sec and block transfers at 37½M bytes/sec. Its minimum transaction time is 200 nsec. Data transfers can include 32-bit words, 16-bit half words, byte transfers, and block transfers of as many as 16 words.



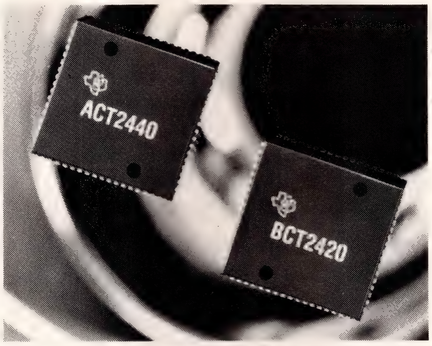
***Sporting sockets for three daughter boards,*** *the MacAdios II lets you convert your Macintosh II to a laboratory computer system; this board records 25,000 samples/sec on one channel while sendng the plot to the Macintosh's screen.*

### Beware of design errors

To ensure that your interface will perform in accordance with the outlined specifications, you must approach the design task with caution. First on the list of pitfalls that you must watch out for is failing to verify that the board can decode attention cycles. The P-1196 spec describes four types of attention cycles: attention-null; attention-resource-lock; and two currently undefined, reserved attention cycles.

The attention-null cycle initiates a new arbitration cycle and indicates the end of a locked-resource transfer sequence. The attention-resource-lock cycle blocks a local µP's access to the slave modules' data resources, thereby preventing a local µP and the bus master from modifying data simultaneously. If you neglect to ensure that a module can decode attention cycles, either the board won't be capable of locking its resources or the module may incorrectly identify the attention cycle as a start cycle and misuse the address released during a lock cycle.

Problems can also occur if you "cheat" on the sample and assert clock edges. The Nubus's 10-MHz clock provides a 75-nsec unasserted (high signal) and a 25-nsec asserted (low signal) duty cycle. This asymmetrical duty cycle prevents bus-skew problems by providing 25 nsec between the sample and driving edges and by allowing 75 nsec for propagation and setup. The bus signals typically change on the rising edge, and the bus master samples on the falling edge. However, if you "cheat" and use the same logic circuit to decode both the sample edge and the assert edge, an error may occur and result in misread data.




***Off-the-shelf chip-set interfaces for the Nubus,*** *such as these developed by Texas Instruments, can dramatically reduce your interface design cycle, but may diminish your application's performance.*

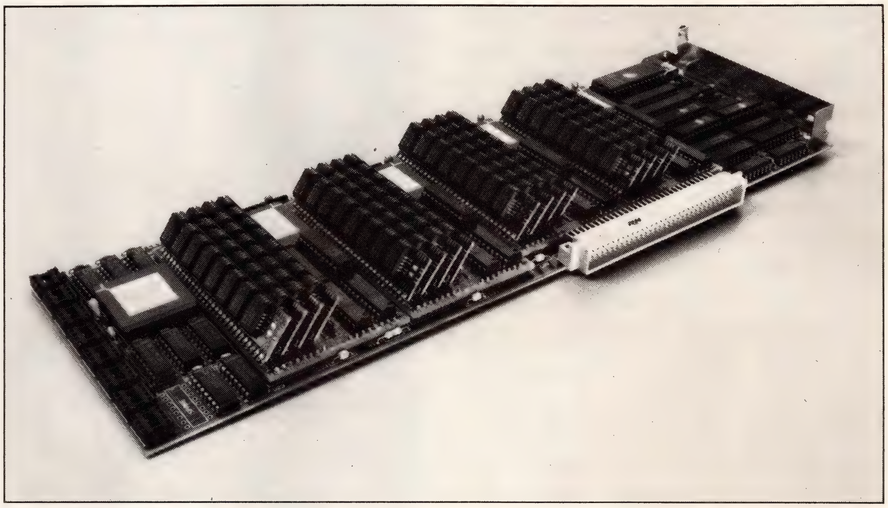
You must also make sure that the bus owner always drives the acknowledge (ACK) signal high at the end of each data transfer. Because bus arbitration occurs in parallel with the Nubus's data transactions, as soon as one bus master completes its transaction, a new master immediately assumes control of the bus. This arbitration technique lets the Nubus use the bus bandwidth efficiently. If poor design techniques

## Nubus interface options

prevent the bus master from driving the ACK signal high at the end of the data transfer, the termination resistor will eventually make the ACK signal go high.

If the backplane is sparsely populated, you may be able to depend on the natural tendency of the ACK line to go high on its own, thereby reducing the logic requirements for the bus master. However, the greater the number of cards plugged into the backplane, the greater the contention for bus ownership and the more critical timing becomes. If the ACK line doesn't go high quickly enough, the boards accessing data on the bus may wind up reading the data twice.

When the backplane is packed with many boards, you must also consider loading violations. The specification permits a maximum of 18 pF of capacitive loading per board for backplanes containing 16 boards. Violating these loading specifications can cause a serious design problem, because the 18-pF limit includes etches and connectors. Multiple onboard drivers also add capacitance. The best way to avoid overloading the bus is to minimize the trace lengths and exercise caution in selecting drivers and receivers.



***The Nubus is designed to expedite parallel processing*** *among multiple µPs. Levco's TransLink is an example of an application that taps the bus's full potential.*

### Weak drivers create havoc

A less common, but equally treacherous design error is the use of weak drivers, such as low-power Schottky (LS) diodes. Although the spec defines a 24-mA dc output drive current, which is well within the capability of an LS device, the ac drive spec is 80 mA. The circuit may operate with a backplane that has few boards, but in a fully loaded system with 16 modules, the LS drivers may not be able to drive the required 15-nsec setup time. Using advanced Schottky (AS) devices will prevent this problem.

If you're designing a Nubus interface for the Macintosh II, which offers only six slots for expansion boards, you many be tempted to use the LS devices because the computer can't hold a fully loaded system. However, at least one company, Second Wave, sells an expansion chassis that adds eight additional slots to the computer's standard capacity. The Expanse II is a \$2295 chassis that includes Nubus interface cards, a cable assembly, a 130W power supply, a cooling fan, and the hardware to support three internal SCSI devices. Without the interface boards, the chassis costs \$1595. For \$2295, the company offers a 4-slot, Nubus expansion chassis for the Macintosh SE/30 computer.

If you assume that your board will be used only in a 6-slot Macintosh II system, you also subject the board to the problem of incomplete address decoding. Boards designed according to the Macintosh II's parameters can decode only six 24-bit, 16M-byte slot addresses. However, when developing the Macintosh II, Apple Corp went beyond the typical P-1196 Nubus spec by including a *super-slot space*. This slot provides an additional 256M bytes per slot. In addition, although the Macintosh II currently uses a 24-bit addressing mode, the company may upgrade the computer to a full-fledged 32-bit machine in the future. If you limit your cards to the Macintosh II's present design, rather than designing to the full parameters of the Nubus spec, you'll shorten your boards' market life.

Also note that Apple isn't the only manufacturer selling a Nubus computer. Texas Instruments markets a \$49,900 Nubus-based LISP workstation called the Explorer II and a \$39,995 multiuser, Unix-based Nubus mainframe called the System 1500. These computers use the triple-height ($11.024 \times 14.437$-in$^2$) expansion boards that were originally defined in the Nubus spec. TI also sells the \$14,995 microExplorer computer, which is actually a Macintosh II with a LISP coprocessor board plugged into it.

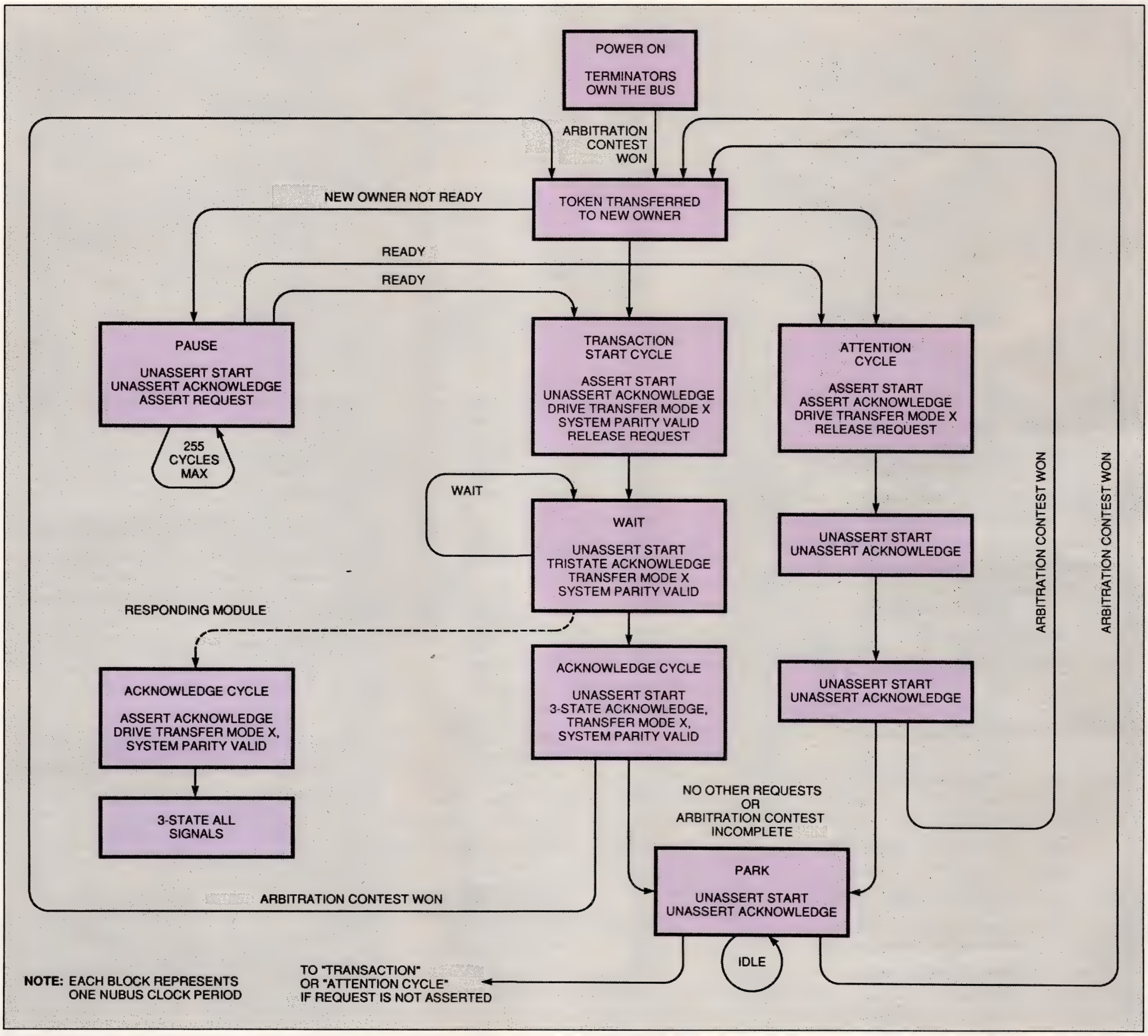
The final design *faux pas* involves data-integrity problems. Such errors will occur if you don't include logic circuitry that will drive the Start line high after an attention cycle. Data-integrity problems also arise when the circuit fails to drive the transfer-mode (TM) lines high during block transfers.

### Nubus interface options

The easiest way to interface a board you've modified for the Nubus is to use a prepackaged Nubus interface chip set, such as TI's ACT2440 controller IC and BCT2420 tranceiver IC. These chips contain the embedded logic necessary to implement the Nubus protocol; they replace as many as 45 discrete logic devices. As a result, they give you as much as 66% more pc-board space, which you can use to add more functions and on-board memory to your module. The ACT2440 sells for $24, and the BCT2420 costs $13.33 (1000). You need two BCT2420 ICs per interface.

These off-the-shelf interface chip sets ensure conformity with the P-1196 spec and can greatly shorten your design cycle. However, many board manufacturers allege that you can't take full advantage of the Nubus's performance when you use the TI chip set because it introduces a wait state. TI could have minimized this delay by using bipolar instead of CMOS technology. The tight 2A Nubus power constraints, however, precluded such a choice.

If your high-speed application can't tolerate the 20-nsec propagation delay introduced by the TI chip set, you can create your own discrete interface by using 7½-nsec PALs. Another alternative is to make the Nubus interface part of a kernel in an ASIC chip that also



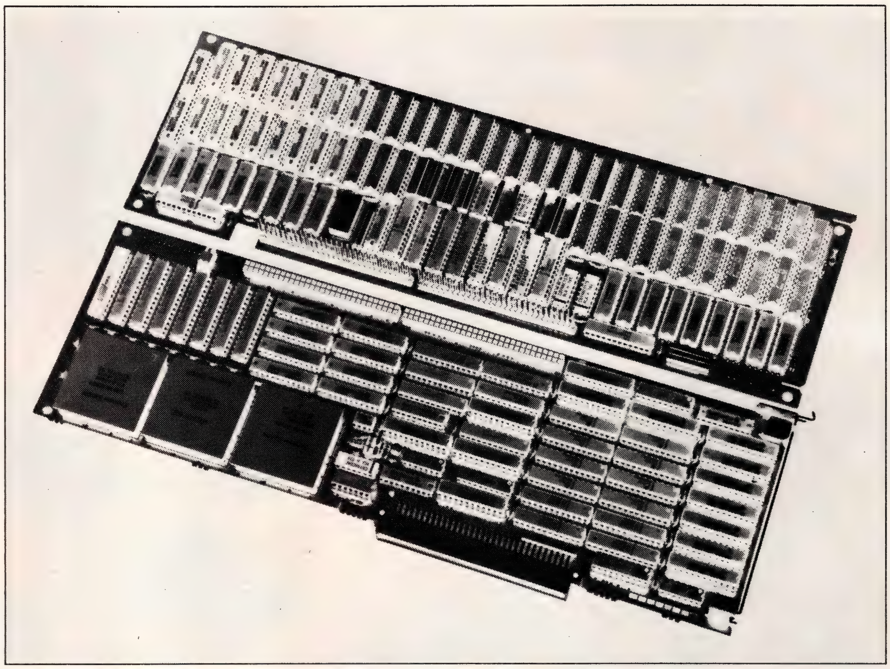

***This flowchart illustrates the signal-driving responsibilities of a bus owner.*** *Each block represents one Nubus clock period.*

**Nubus interface options**

includes a portion of the module's logic.

The TI chip set not only introduces a wait state, but also lacks direct support for Nubus master block transfers. Therefore, you must use external logic to allow your module to read and write block data.

One benefit of block mode is that it doubles the data-transfer speed. In addition, the data bursts lower the bus bandwidth consumption, resulting in less bus arbitration. However, Apple didn't design a block mode for the Macintosh II, and the external logic needed for block data transfer requires the fastest and most expensive FIFO memories available.



***By implementing block-mode data transfers on a bus-master board,*** *Mercury Computer Systems' MC-3200NU coprocessor board can reach 20M flops in a Macintosh II.*

### Nubus boards ready for action

To bypass many of the headaches associated with designing your own interface, you can choose from a variety of Nubus-compatible boards. Mercury Computer Systems, for example, offers a processor card that integrates bus-master and block-mode capabilities in one board. This single-slot processor card, which was introduced at Siggraph '88 (Atlanta, GA), features 20M-flops and 10-MIPS performance. When coupled with a module that has similar data-transfer specs, the MC3200NU can transfer data at a rate of 30M bps in block mode. This transfer rate lets you perform computation-intensive vector and scalar operations, such as those used in simulating, modeling, signal processing, image processing, and Postscript manipulating. The card's nonblock transfer rate can reach 10M bps. Also, the card can transfer data to and from the Macintosh II's memory at a rate of approximately 5M bps. With 2M bytes of memory, the MC3200NU sells for $10,000; the Fortran and C software development package costs $8500.

Another high-performance coprocessor board for the Macintosh II is Yarc Systems' NuSuper module. Sporting a 25-MHz Am29000 RISC μP and offering an optional Am29027 floating-point coprocessor, the NuSuper module features a peak 25 MIPs, more than 25,000 Dhrystones, and 3M Linpack performance. The $4000 NuSuper

## Avoid Nubus design errors

According to Gerry Laws, Chairman of the NuGroup (Tustin, CA, (714) 669-1201, FAX 714-669-9105), the most common design errors made by developers of Nubus interfaces include:

- Neglecting to make sure the board can decode attention cycles,
- Cheating on the sample or assertion edges,
- Failing to ensure that the bus owner drives the acknowledge signal high at the end of a data transfer, and
- Violating loading specs.

Other potential design errors include:

- Using weak drivers,
- Designing for a 6-slot board instead of a 16-slot board,
- Failing to drive TM 0/1 high during block transfers,
- Neglecting to decode the address completely, and
- Not driving the start line high after an attention cycle.

**Nubus interface options**

board operates in parallel with the host μP and offers transparent background computations. A C compiler is now available for the board, and a Fortran compiler will probably surface during the second quarter of this year.

**Wire-wrap your design**

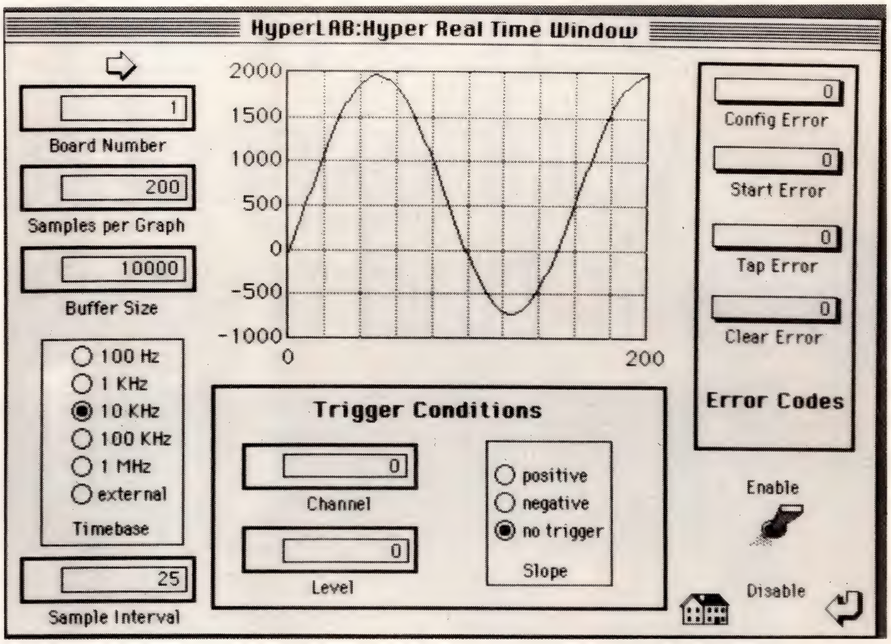
Creative Solutions also offers an alternative to designing your own interface for the Nubus. The vendor's Nubus Hurdler is an interrupt-driven Nubus slave interface on a Macintosh II card with an 894-pin wire-wrap area. Selling for $279, the Hurdler includes a slot-declaration ROM, as required by the P-1196 spec. It also comes with three 16-bit counter/timers, a software driver, and application notes. For $199, you can purchase an interface that lets you connect the Macintosh II to a Centronics printer, or, for $349, you can buy an interface that lets you plug the Hurdler into an IBM PC bus.

If you're interested in performing high-speed parallel processing on your Macintosh II, consider Levco's TransLink board. It lets you tap the RISC (reduced-instruction-set computer) technology of an Inmos Transputer. The starter kit, which sells for $2597, includes a TransLink board with 1M byte of RAM, an assembler, and C. You can purchase the Occam II Transputer programming language and a Transputer development system for $1200.

Several Nubus boards, such as National Instruments' NB-MIO-16X 16-bit A/D converter, are suitable for data-acquisition applications. The 42-μsec version costs $1695; the 18-μsec board sells for $1895 and offers a guaranteed data rate of 55 samples/sec. For $1195, you can buy a 12-bit NB-MIO-16 multifunction board.

National Instruments also provides software support with its $295 NB-LabDriver software and $1995 LabView instrumentation software package, which comes with a free library of virtual instruments that you can use with the board. LabDriver also includes a language-interface library for Lightspeed Pascal and a HyperTalk interface with Hypercard stacks. LabView provides a graphical programming platform that has analysis and graphical-presentation tools, with which you can rapidly develop programs to acquire, control, process, and display signal information.

GW Instruments offers six Macintosh II data acquisition boards, including the MacAdios II. This card simultaneously records one channel at 25,000 samples/sec and sends the plot to the Macintosh's monitor screen. Its 5-μsec A/D converter has a throughput specification of 142,000 samples/sec. A 12-bit A/D converter, two 12-bit analog output channels, eight digital I/O channels, three counter/timer channels, and three A/D trigger modes come with the $1490 board.




***Many Nubus-board manufacturers have developed software elements*** *that ease the development process. National Instruments' NB LabDriver, for instance, provides a graphical interface that simplifies the task of building customized data-acquisition processes.*

You can plug three daughter boards into the MacAdios II to expand its capabilities with antialiasing filters, a time stamper, and as many as 96 additional analog inputs. The daughter boards range in price from $65 for the Protoboard to $1425 for the 1-channel, 12-bit A/D converter with an 833-kHz maximum sampling rate. For $190 you can purchase TurboDrivers, which you can access from seven languages, including C, Pascal, Fortran, and QuickBasic.

Strawberry Tree Computers offers a line of eight Macintosh data-acquisition boards, including the 12-bit, 8-line A/D plug-in board (ACSE-12-8) for the Macintosh SE and the 16-bit, 16-line board (ACM2-16-16) for the Macintosh II. The ACSE-12-8 sells for $595, and the ACM2-16-16 costs $1845. The boards offer self-calibration and self-diagnostic capabilities and fea-

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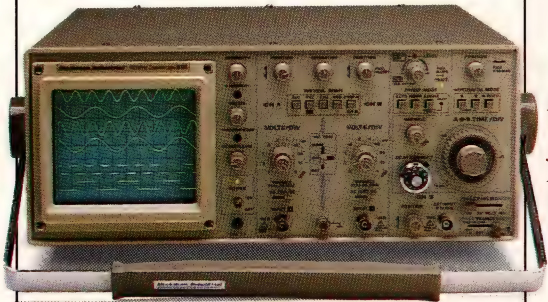
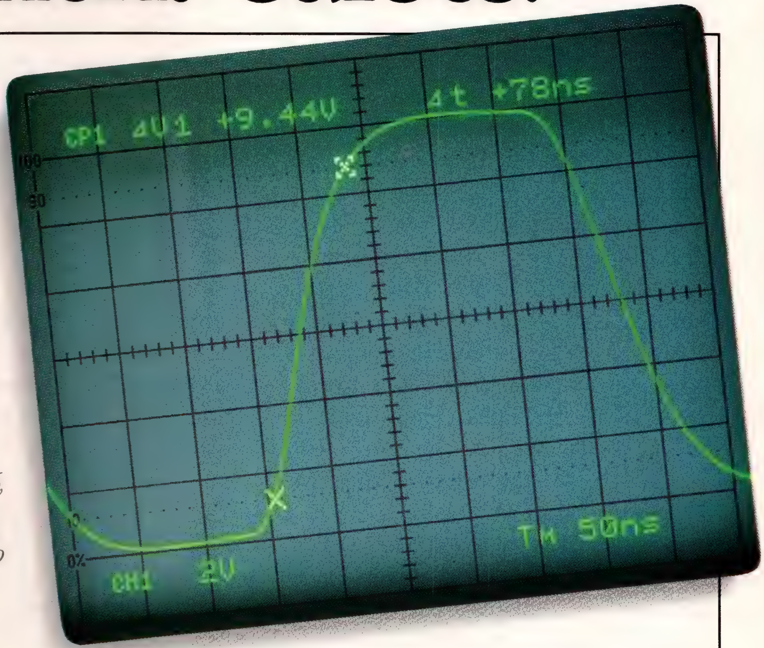


*Model 9106, 60MHz, 3 Channel, Dual Sweep (A & B).*

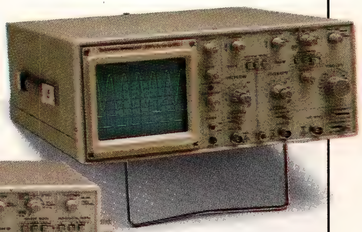



*Independent cursors and on-screen readouts make waveform measurements fast and accurate.*

Five of six models feature two independently-adjustable time bases. Built-in intensity modulation allows you to select a small section of a main waveform for closer examination. This feature is ideal for measuring pulse rise times or checking sync pulse amplitudes in composite video signals.

*Model 9204, 40MHz, On-Screen CRT Readout.*

*Model 9104, 40MHz, 2 Channel, Dual Sweep (A & B).*



*Model 9022, 20MHz, 2 Channel.*

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## Solid Design.

The Series 9000 features a low-profile cabinet, logically grouped controls, camera-mount CRT bezel and graticule illumination for waveform photography. Most models feature a three year warranty.

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| FEATURES | 9106 | 9104 | 9204 | 9202 | 9102 | 9022 |
|---|---|---|---|---|---|---|
| Max Frequency | 60MHz | 40MHz | 40MHz | 20MHz | 20MHz | 20MHz |
| Input Channels | 3 | 2 | 2 | 2 | 2 | 2 |
| Dual Sweep (A & B) | • | • | • | • | • | |
| CRT Readout | | | • | • | | |
| Cursor Readout | | | • | • | | |
| Switchable X1/REF/X10 Probes | 2 | 2 | 2 | 2 | 2 | 2 |
| Warranty | 3 year | 3 year | 3 year | 3 year | 3 year | 1 year |
| Price | $1,290 | $950 | $1,095 | $865 | $700 | $550 |

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CIRCLE NO 111

**Nubus interface options**

ture a data speed of 2500 to 20,000 samples/sec. The Analog Connection WorkBench application software, which costs $495, provides an object-oriented graphical interface that lets you easily develop programs for your data-acquisition and -control applications.

If you're designing for the Macintosh II and you want to be able to plug IEEE-488 data into a Macintosh-based application such as a spreadsheet, you can use IOtech's MacII488 card and MacDriver488 driver software for Basic, Pascal, C, and other languages. Selling for $595, the MacII488 comes with a desk-accessory program called MacDA488, which lets users plug IEEE-488 data directly into your spreadsheet. The board transfers data at speeds as fast as 600k bytes/sec.

Whether you'll use these Nubus-compatible expansion boards or design your own Nubus interface depends largely on your application and your design goals. If, for example, your work involves mainly data-acquisition applications, buying an expansion board may be the simplest solution. However, if your applications are more varied and complex, you may not be able to find a ready-to-use Nubus board that meets your needs. If the demand for Nubus computers should increase dramatically in the near future, you may have even more design and product options to choose from, which will greatly simplify your interfacing task. At present, though, it's too early to tell whether that demand will increase significantly. EDN

## References


1. *Nubus—A Simple 32-bit Backplane Bus*, P-1196 Specification, Draft 2.0, December 15, 1986.
2. Harvey, Audrey, "Simple circuitry connects plug-in cards to Nubus," *Electronic Design*, February 18, 1988, pg 97.
3. Marshall, Trevor and Jim Potter, "How the Macintosh II Nubus Works," *Byte, Second 1988 Mac Special Edition*, December 1988, pg Mac 39.


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## For more information . . .

For more information on the Nubus products discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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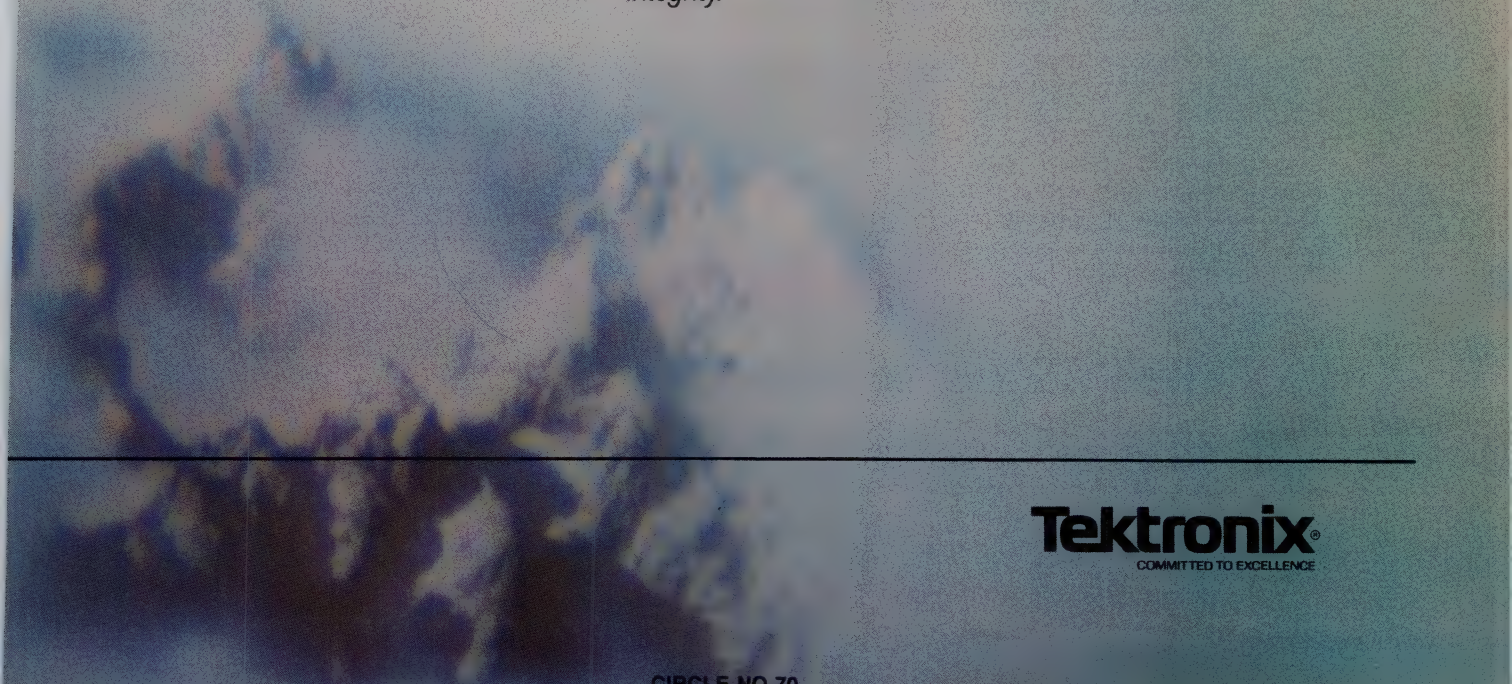

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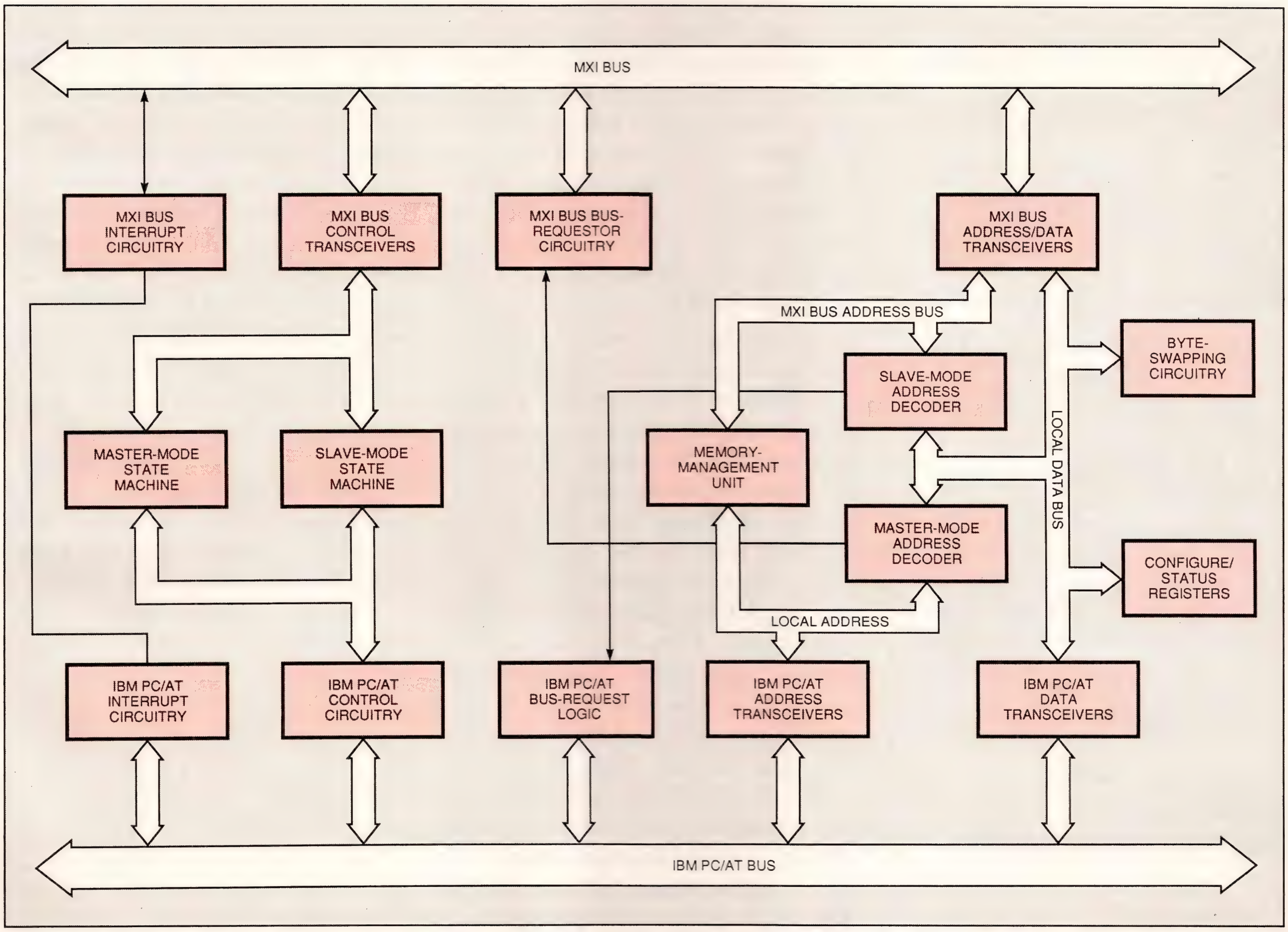
# VXI Bus enhancement accommodates physical instruments and multiple mainframes

The MXIbus (pronounced MIX-ee-bus) is an enhancement of the VXI Bus, which is well known among system developers for its high-performance, instrument-on-a-card architecture. MXIbus lets you daisy-chain and multidrop mainframes full of card-bound instruments, and even lets you add full-size physical instruments and PCs to your VXI Bus system.

MXIbus—an acronym for Multisystem eXtension Interface bus—provides a 32-bit, multimaster, frame-to-frame interface that lets a single VXI Bus resource manager configure your entire multiframe system. It provides word-serial drivers and utilities that let the resource manager identify all the devices in the system, manage the system's self tests, configure the A24 and A32 address maps, establish the initial system hierarchy for multimaster arbitration, and initialize normal system operation. It also defines a method for extending TTL triggers, VME interrupts, CLK10, and SYSFAIL across multiple frames.

Incorporating a backplane-bus-on-a-cable design, the MXIbus assigns VXI Bus logical addresses to the physical devices connected to the bus. Its multidrop parallel bus architecture provides a way to couple a VXI Bus tightly to external industry-standard personal computers, such as the IBM PC/AT, PS/2, Macintosh, and EISAbus machines, and to instruments that will never physically fit on a VXI module. With the MXIbus and a PC, a VXI Bus system developer can use industry-standard software to speed




***Providing an operational link among multiple VXI Bus mainframes,*** *physical instruments, and the IBM PC/AT bus, National Instruments' MXIbus lets you control as many as 256 devices in a multidrop, parallel-bus architecture.*

# PRODUCT UPDATE

development tasks.

By mapping together portions of each device's address space and interlocking the internal hardware bus cycles of the devices linked to the bus, MXIbus accommodates 8-, 16-, and 32-bit data transfers, block-mode transfer for sustained data rates approaching 20M bytes/sec, and inseparable read-modify-write operations. The 62-pin MXIbus connector encompasses 49 active signals (including 32 multiplexed address and data lines with parity), address modifiers for multiple address spaces, single-level multimaster prioritized bus arbitration, interrupt capability, bus-error handling of timeouts and deadlock conditions, and handshake lines for asynchronous operation.

Because MXIbus doesn't specify what you can attach to it, it is more of a general-purpose bus than the instrument-specific GPIB. Thus, you can tap the data flow from high-speed input devices such as optical scanners without facing the bottleneck posed by protocol-laden links.

Each MXIbus interface has address-window circuitry that monitors both the internal local address lines and the MXIbus lines. This circuitry detects the occurrence of an internal bus cycle that maps out to the MXIbus; it also detects when a MXIbus cycle's address is mapping into the internal system. The interface interlocks the local bus cycle to the MXIbus and initiates a MXIbus cycle to the specified address. Optional address-page registers permit the address windows to occupy only a small portion of the local address space. You can move the address windows to access the full MXIbus 32-bit address space by changing the page register values.

The MXIbus does not, however, accommodate system architectures in which nodes are connected in a ring. Neither does it extend the VXI Bus' Analog Summing Bus, the Local Bus, CLK100, SYNC100, ECL triggers, or Star triggers. And, although National Instruments has distributed a proposed specification for its MXIbus among the members of the VXI Bus consortium, no formal recognition has yet occurred.

To support the proposed MXIbus standard, the company has introduced the MXI-VXI and AT-MXI interfaces. The $1995 MXI-VXI board is a C-size VXI module with slot 0 capability. You can connect as many as 32 VXI mainframes to operate as a single VXI system with 512 slots and a common address map. A 2-meter MXIbus cable costs $300.

The $995 AT-MXI board links an IBM PC/AT to one or more VXI Bus mainframes via the MXIbus. The PC/AT treats each VXI Bus chassis and its internal instrument cards as though they were plugged directly into the backplane of the PC/AT. The chassis communicate via VXI protocols. The AT-MXI interface handles the bus cycle translations, performs shared-memory data transfers, and includes VXI Bus Resource Manager software and VXI word-serial device drivers. Although embedded PCs-on-a-board are currently available for the VXI Bus, you may find the combination of an AT-MXI board and your own PC to be a more cost-effective and versatile solution.

***—J D Mosley***

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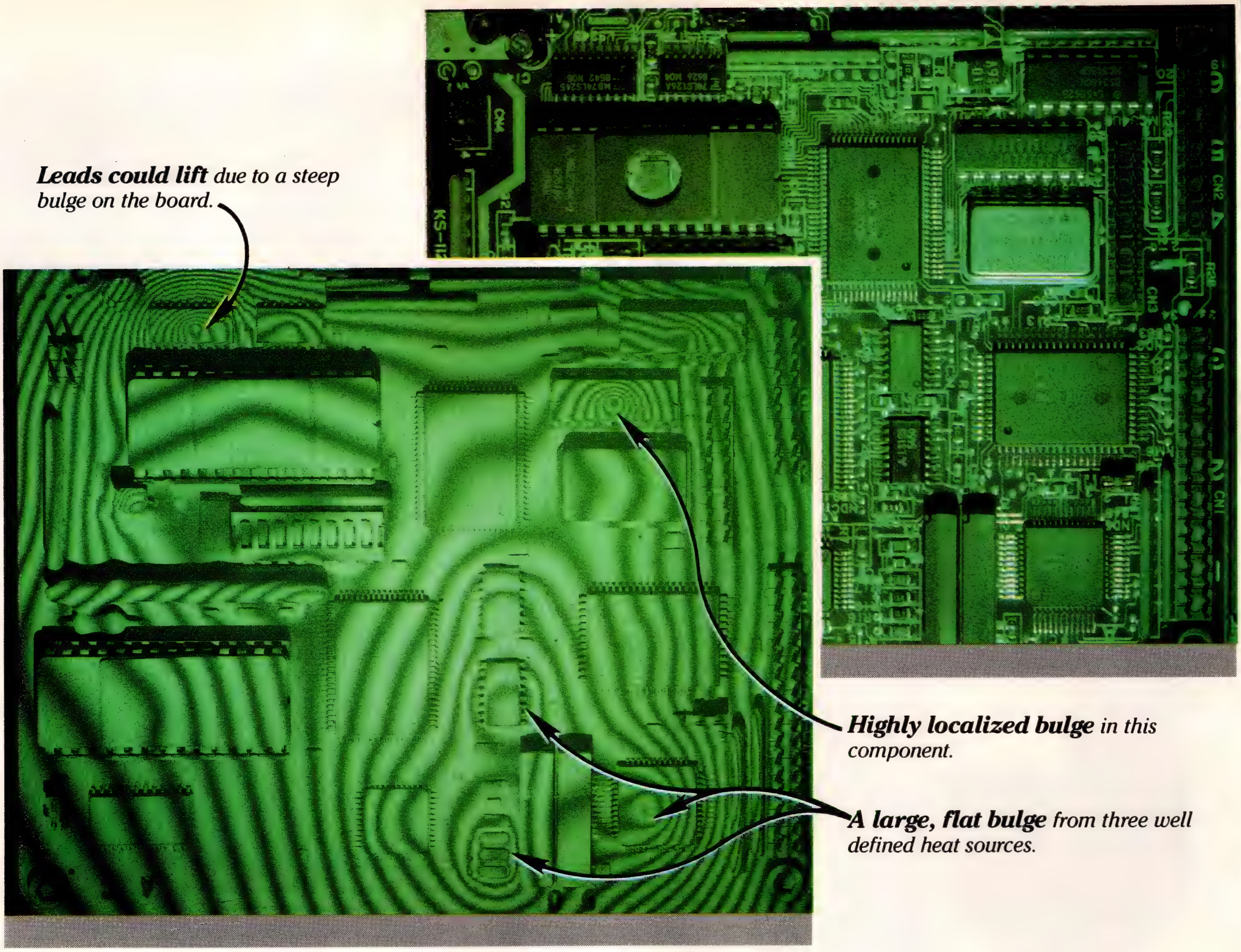
**Circle No 735**

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# 32-bit Ethernet controller chip maintains layer-management statistics

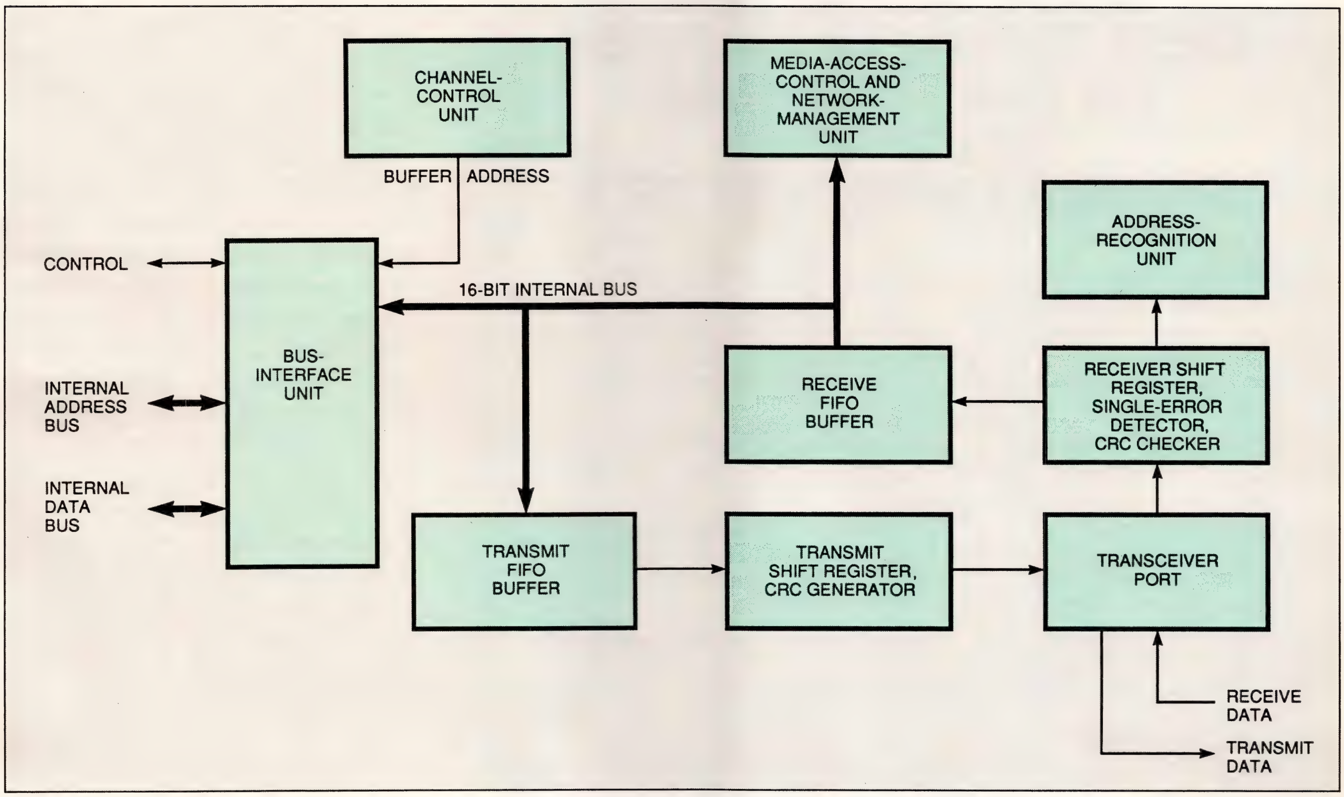
Although a latecomer to the LAN-controller market, the 92C28 Ethernet controller chip promises to deliver unusually high system performance through its 32-bit interfacing capability. The $35 (5000) device can operate as a local bus master or as a slave to a host μP, and it maintains a full complement of network statistics as defined by the IEEE-802.3 layer-management draft specification. In addition, the company created the device using design rules that are compatible with its 1.5-μm ASIC fabrication process and can therefore develop alternative versions of the controller for interested customers.

Internally, the 92C28 employs a 16-bit architecture, which is apparent from the device's 16-bit address and data ports. You can connect the IC to a host μP as a slave device, using either a memory-mapped or an I/O-mapped interface—the chip has control pins for both interface types. The I/O-mapped interface allows a low-cost, low-performance approach to LAN node design that uses the host CPU's memory for transmit and receive buffers. The memory-mapped interfacing scheme allows you to attach local memory to the LAN controller so that it can automatically manage its own buffers, thus achieving somewhat higher performance. The chip can also share its buffer memory with a μP through a DMA request/acknowledge protocol.

Through multiplexing, you can adapt the 92C28's 16-bit data bus to a 32-bit system. You must add external latches and transceivers to hold the incoming and outgoing 32-bit data words because the controller can only transfer 16 bits/clock cycle. However, the controller generates all necessary latch strobes and transceiver enables to ease this design approach.

This 32-bit interface not only improves the match between the LAN controller and a 32-bit μP, but it also boosts system performance by raising the maximum data-transfer rate to 20M bytes/sec, a 50% increase over the rate obtainable with the chip's 16-bit mode. You may not need this additional bandwidth to service a 10M-bps Ethernet LAN, but the higher transfer rate can free the μP's bus for other processing chores not related to network traffic.

The Ethernet controller's 32-bit




***Although it has a 16-bit architecture internally,*** *the 92C28 Ethernet controller can operate in both 16-bit and 32-bit systems.*

mode provides yet another advantage: It supports 256k bytes of buffer RAM compared with only 128k bytes for the 16-bit mode. You may need this additional storage for very active LAN devices such as file servers. For packet transmissions, the controller employs a chained, dual-buffer scheme, and for incoming packets, the chip employs a ring buffer. You program the addresses of the various buffer areas through six pointer registers in the controller.

The 92C28 maintains several network performance statistics in on-chip registers. The registered transmission statistics include the number of frames transmitted properly, the number of single- and multiple-collision frames, the number of octets transmitted properly, the number of deferred transmissions, and the number of multicast and broadcast frames transmitted properly. Registered receive statistics include the number of properly received frames and octets and the number of properly received multicast and broadcast frames. In addition, the chip records several other error statistics relating to the transmitting and receiving of packets.

Maintenance of network statistics at each LAN node can potentially help a network manager achieve maximum throughput and reliability in an Ethernet LAN, provided designers make the statistics accessible when designing node equipment. The 92C28's statistics registers implement the functions listed in the IEEE-802.3 layer-management draft specification, thus encouraging you to integrate layer-management functions in your Ethernet designs.—***Steven H Leibson***

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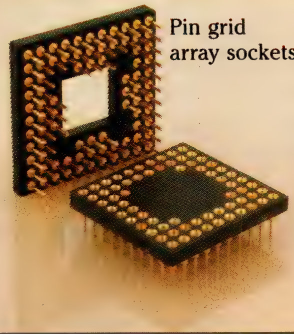

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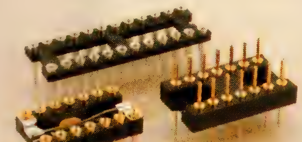

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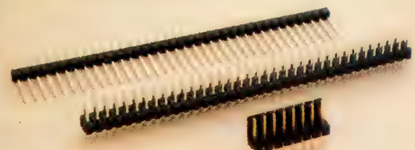


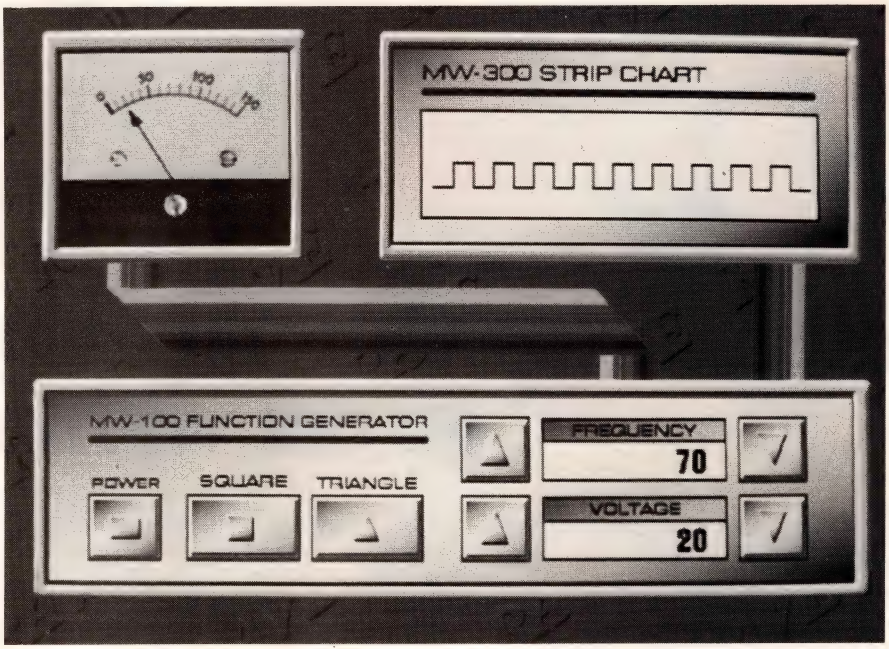
# Development tool simplifies the creation of user interfaces for real-time systems

The Rave (Real-time Audio/Video Environment) software-development tool simplifies the design of human interfaces for real-time applications such as those for process-control systems. The development tool is an extension of the OS-9 real-time operating system and allows you to combine audio, video, computer-generated graphics, and customizable menus in creating a user interface.

You can use Rave to create interfaces for real-time systems that nontechnical operators intuitively understand. Furthermore, you can develop a custom audio/video user interface without writing a single line of code.

Three software packages make up the Rave development tool: the Graphics File Manager, the Graphics Support Library, and the Presentation Editor. The Graphics File Manager provides the audio, video, and input drivers needed to support the run-time user interface. For example, the input drivers provide support for a standard keyboard, a keyboard customized for a specific application, and pointing devices such as a mouse, digitizing pad, or touch screen. The video driver supports a monitor and provides drawing and block copy primitives.

The Graphics Support Library builds on the Graphics File Manager and includes the menus, controls, and indicators employed in a user interface. For example, controls are objects on the display that mimic the behavior of switches or slidebars. Likewise, indicators mimic the behavior of devices such as meters, LEDs, and strip-chart recorders. The Graphics Support Library includes a number of standard controls and indicators, and you can also build custom controls and indicators.




***A sample screen of a typical user interface*** *demonstrates the intuitive visual effect that Rave-based applications project.*

You use the menu-driven Presentation Editor to actually develop a user interface. The keyboard and the mouse let you interact with the Presentation Editor, thereby creating the user interface based on the controls, indicators, and menus supported by the Graphics Support Library. You can input audio to the Presentation Editor directly from a microphone or from a disk. You can use a camera to capture the video or build it from graphics primitives. A paintbrush facility allows you to modify computer-generated or real-world video images.

Currently, Rave supports a frame-grabber board, an audio I/O board, and a speech chip, but you can easily add support for any audio/visual product by developing drivers for the Graphics File Manager. You can also expect a number of CPU-board manufacturers that currently support the OS-9 operating system to support the Rave extension as well.

The three partitions of Rave are separately priced: Graphics File Manager, \$300; Graphics Support Library, \$175; Presentation Editor, \$995. You may only need a single copy of the Presentation Editor to develop products, but you may also need to ship a copy of the run-time Graphics File Manager or the Graphics Support Library with each system you ship. All the units are scheduled for release in mid-May.

***—Maury Wright***

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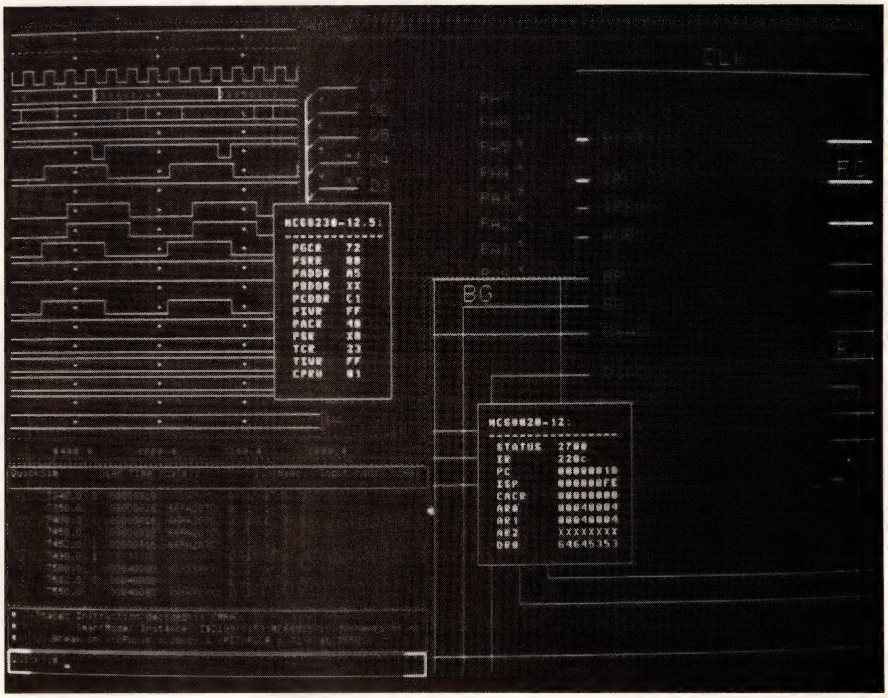
# Software-modeling capability allows you to "emulate" your system designs

You can now simulate your system designs, using Mentor Graphic's QuickSim simulator in conjunction with SmartModel Windows, a behavioral software-modeling capability. SmartModel Windows can actually look inside the registers of the models of processors, peripherals, PLDs, and memories during simulation. This capability lets you build, simulate, emulate, and debug the system before you prototype your designs.

Emulation has always been a useful technique for evaluating your designs involving µPs. You could use an emulator to debug both the hardware and software of your system designs by single-stepping through the program and examining the data in registers internal to the µP. When you finished the process, you'd just replace the emulator with the actual microprocessor. But you could only do this at the hardware level.




***You can single-step your hardware design** through your program and examine the registers at each step. Here, SmartModel Windows models emulate a system controlled by an MC68020 µP and containing an MC68230 parallel interface/timer. They're shown with the Motorola chips' internal-register values that are available for examination.*

SmartModel Windows provides internal register visibility for some Motorola processors and peripherals, including the MC680X0 family, the MC68230, MC68440, MC68442, MC68452, MC68851, MC68881, and the MC68HC11. You can also use SmartModel Windows for PLDs from AMD/MMI, Altera, Lattice, and Texas Instruments. By July, the vendor is planning to provide SmartModel Windows for a range of Intel devices, and by the end of the year, for most devices in its SmartModel library that have internal registers.

SmartModel Windows is tightly coupled with the simulator's user interface, thereby letting you work with the SmartModel's internal registers exactly as with the external nets of the design. If the simulator supports SmartModel Windows, you can single-step, set breakpoints on internal-register states, or set internal-register values. In addition to Mentor's QuickSim, the vendor is working to couple SmartModel Windows with HP's Electronic Design System.

You can get SmartModel Windows as an option to the vendor's 1-year subscription service for the SmartModel library of more than 4000 devices. Subscribers receive quarterly updates containing all new models and, if you order the SmartModel Windows option, you will receive the Windows capability for each new set of devices as they are released. The SmartModel's subscription service is $7900 per workstation, and the SmartModel Windows option costs an additional $4000.—***Michael C Markowitz***

*Logic Automation Inc, 19500 NW Gibbs Dr, Beaverton, OR 97075. Phone (503) 690-6900. FAX 503-690-6906.*

**Circle No 733**

# Color LCD panel uses TFT technology to achieve high contrast and sharpness

***Active-matrix TFT technology*** *enables this LCD panel to reproduce eight colors that have high contrast and 640×(200×3) pixels of resolution.*

Reproduced here, the color transparency cannot do justice to the brightness, contrast, sharpness, and vibrancy of the company's TFT (thin-film transistor), 6.3-in., 8-color LCD display. You really have to view the actual display to appreciate its visual impact.

Using amorphous silicon TFTs in an active-matrix arrangement, each pixel in the display is driven by its own transistor. Individual red, blue, and green color filters over each pixel make the 8-color operation possible. Deleting the color filters yields a high-resolution monochrome display having all the advantages of TFT technology. Both the color and monochrome displays typically employ a fluorescent backlight.

Although the interface circuitry for the TFT display is multiplexed, when examined at the individual pixel level the display actually is statically driven by the individual TFT drive circuits. This arrangement preserves the simplicity of designing in a multiplexed display and eliminates the resolution vs contrast tradeoff normally associated with other LCD technologies.

The thin-film transistors are FETs. The drain leads of the FETs are connected to form column-selecting terminals; the gate leads are connected to form row-selecting terminals. When the display selects a particular pair of row-column terminals, that individual FET turns on, activating the LCD pixel connected to that FET's source lead. Compared with previous LCD technologies, this configuration provides higher resolution, improved brightness and viewing angle, and significantly improved contrast and speed.

The extremely sharp image quality of TFT technology results from the fact that when the display is passing light, the light passes straight through without any defocusing on the pixel edges. By contrast, other active displays such as CRTs and emissive flat panels appear less sharp because the emitted light travels in several directions simultaneously, resulting in an apparent defocusing of the image.

Although this LCD panel is quite expensive ($700 in OEM quantities), it has some impressive specifications. The effective display area is 96×128 mm. The resolution is 640×(200×3) pixels for color and 640×600 pixels for monochrome, totaling 384,000 pixels. The contrast ratio is very high at 40:1. The viewing angle of ±45° lets you see what's on the screen without having to look at it head on, and the display's 40-msec response time is suitable for mouse-driven applications. The LCD panel operates from 5 and 25V supplies, and power consumption is only 5W with backlight and 1.5W without backlight.

Though the display's present high cost precludes its use in most low-end applications, other applications such as medical instrumentation, avionics, and high-end portable computers would likely benefit from the use of a compact, low-power, full-color display. And, as production yields improve and costs go down, you'll likely find these displays among lower-cost consumer products.—***Dave Pryce***

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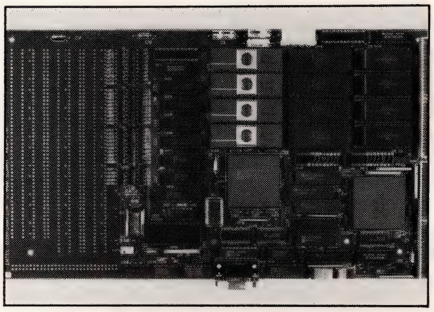
PHILIPS

# Prototyping board kits include a RISC-like µP

The two EVQT960 µP-board kits provide designers with a low-cost way to evaluate or prototype products based on the company's 32-bit, 20-MHz 80960KB RISC-like processor. The kits include working CPU boards, schematics, programmable logic equations, and a software-debug monitor. The CPU boards include an onboard prototyping area and a connector that you can use to add more circuits off board.



***The 20-MHz 80960KB-based CPU boards included in the EVQT960E/F*** *evaluation and prototyping kits allow designers to quickly develop hardware and software based on the new RISC-like embedded controller.*

The 80960KB currently tops the company's embedded-controller product line. The µP includes an integrated floating-point unit, instruction and operand caches, and an on-chip interrupt controller. The processor also supports a burst mode for fetching instructions and data, and the boards included in the prototyping kit employ interleaved memory to support the burst mode.

You can choose from kits with slightly different 80960KB-based boards. The EVQT960F20 kit costs \$1960 and includes 128k bytes of zero-wait-state static RAM and 128k bytes of flash EPROM installed on the CPU board. The board included in the \$960 EVQT960E20 kit hosts 128k bytes of 2-wait-state static RAM and sockets for 128k bytes of EPROM. The boards include a programmable wait-state generator that allows you to model different memory-subsystem architectures.

Other board features include an RS-232C port and eight DMA channels. You power the boards with any standard IBM or compatible personal-computer power supply. The prototyping area of the boards has complete access to the CPU core-system buses and signals.

The boards come with the public-domain Nindy debug monitor stored in EPROM. Nindy provides features such as code execution at a specific address, five instruction traces, two hardware breakpoints, display/modify registers, display/modify memory, code disassembly, and code/data download via the RS-232C port.

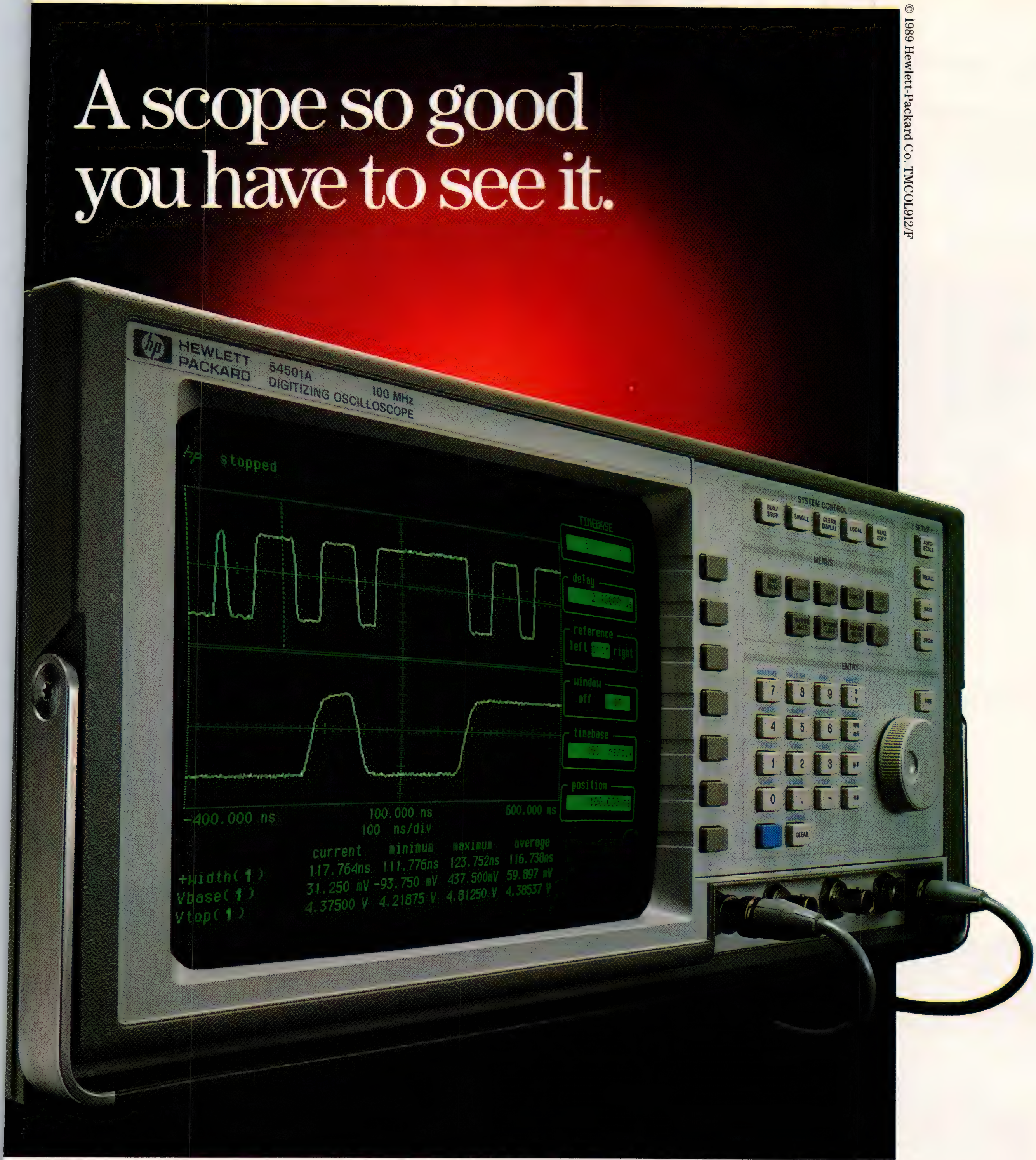
You can communicate with Nindy from a host computer that has a terminal-emulation program and an XModem file-transfer facility. Intel also offers the ASM-960 assembly-language software package, the iC-960 C language software package, and the ICE-960 in-circuit emulator for use with the prototyping kits.

The kits include IBM PC-compatible 1.2M-byte floppy disks that contain a schematic data base of the CPU board, PLA equations, the CPU-board parts list, and source code for the Nindy debug monitor. You also receive an EVQT960 users' manual and power-supply cables in the kit. You can expect shipments of the kits by mid-year.

***—Maury Wright***

*Intel Corp, Dept 9P01, 3065 Bowers Ave, Santa Clara, CA 95052. Phone (800) 548-4725. FAX 408-765-2633.*

**Circle No 732**



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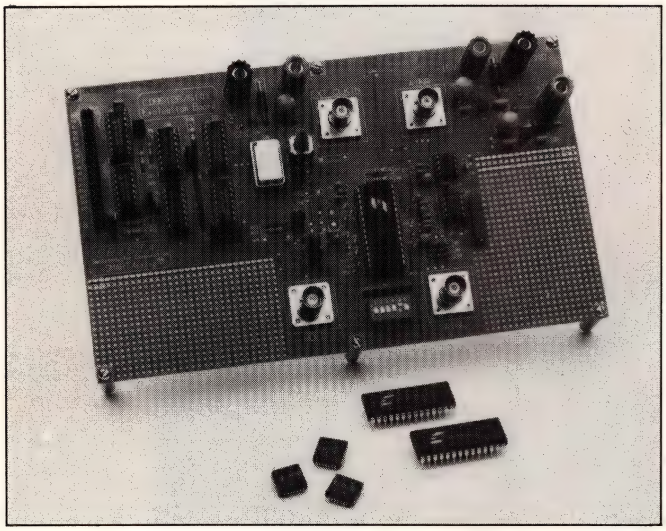
HEWLETT PACKARD

# READERS' CHOICE

Of all the new products covered in EDN's **October 13, 1988,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our **October 13, 1988,** issue.



## ◄ DIGITAL AUDIO ADC

The CSZ5126 is a monolithic stereo A/D converter for use in digital audio applications. The chip features 16-bit resolution and has a 92-dB dynamic range (pg 296).
**Crystal Semiconductor Corp.**
**Circle No 601**

## FAX SOFTWARE

CAD-Fax is a communications package that consists of menu-driven software and a half-size fax modem card that plugs into IBM PCs, PS/2s, and compatibles (pg 311).
**GammaLink.**
**Circle No 604**

## ▲ HANDHELD DMMs

The models 83, 85, and 87 meters are environmentally sealed, handheld units with $3\frac{3}{4}$-digit (4000-count) liquid-crystal displays (pg 301).
**John Fluke Mfg Co Inc.**
**Circle No 605**
**Philips Test and Measurement.**
**Circle No 606**

## ▲ IMAGE SCANNER

The RS320 desktop scanner is capable of scanning sheets, cards, or books at resolutions ranging from 60 to 360 dpi, and can scan a letter-size document at 18 sec/page with 300-dpi resolution (pg 266).
**Ricoh Corp.**
**Circle No 602**

## KEYPAD LEGENDS

This legend label system is available for the company's Series 89 keypads. The labels are available in sheet form with numbers, letters, symbols, and standard key inscriptions (pg 281).
**Grayhill Inc.**
**Circle No 603**

# The plot that took 20 years to unfold.

# How Versatec helped change your picture of the world.

If you've got a plotting problem, chances are the company that can solve it is the one with the longest history of doing just that. That's why we'd like you to reflect on the rather long history of Versatec. Because our past might just have an impact on your future.

### *1969. The revolution begins.*

Woodstock, miniskirts and those amazing Mets. In technology, it was a year filled with excitement. A man on the moon. The jumbo jet and Concorde. The artificial heart.

But there was another event that almost went unnoticed. One that would change forever the way engineers worked. Versatec was formed. And a little while later, we introduced the first 11-inch electrostatic plotter.

While crude by current standards, our first plotter started a revolution in engineering productivity that's still going strong today, 20 years and 50,000 systems later.

In fact, today there are more Versatec electrostatic plotters in more places throughout the world than all other brands combined.

### *1973. The plot widens.*

Watergate hearings. Rabies vaccine. Supermarket scanners. Color copiers. And a new development in engineering that would change the world—computer aided design.

Automotive, architectural, aeronautical and electrical engineers were clamoring for vastly wider plots than anything ever seen before.

Versatec responded with a whole new line of wide carriage plotters. In widths from 20 to a whopping 72 inches. Plus the ability to print on paper or vellum in clear or matte finishes. A little later we'd add 200 ppi resolution, the first RS-232 and direct CRT interfaces, first I/O multiplexer, minicomputer graphics software, universal graphics software and a few dozen other innovations.

### *1976. Supplies meet demand.*

While R2D2, C3PO and the space shuttle were cavorting in space, Versatec announced something a little more down-to-earth. Our very own supplies research group. Dedicated to making sure that our electrographic supplies are as advanced as our plotters, these folks are now responsible for over 50 patents covering a wide range of papers, films, toners and other supplies. And our warehouses in the U.S., Canada and Europe can ship our supplies at a moment's notice.

### *1982. The color purple (and green and blue and yellow).*

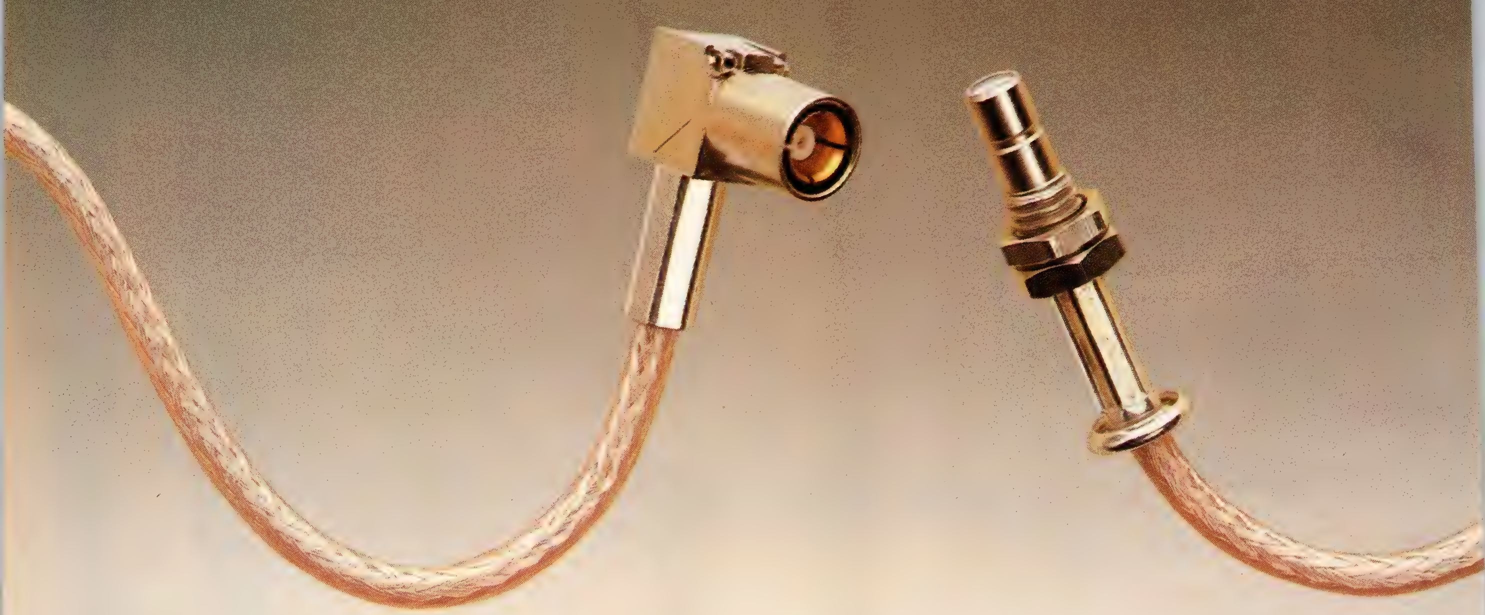
While E.T. and disk cameras were getting lots of attention, we were giving serious attention to R&D. And especially to customers who needed more dimension in their plots.

The result was the world's first electrostatic color plotter. Then we carried that technology even further with second-generation systems in 24, 36, and 44 inch formats. Followed by high resolution thermal plotters in color. And another long list of firsts, including a random element processor, plot server, color plotting software, color toners and media.

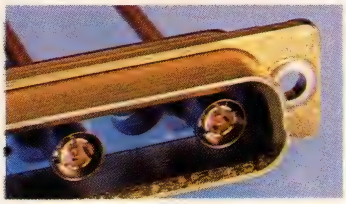
### *1988. Drawing some fine lines.*

We shouldn't have to tell you what happened in the world last year.

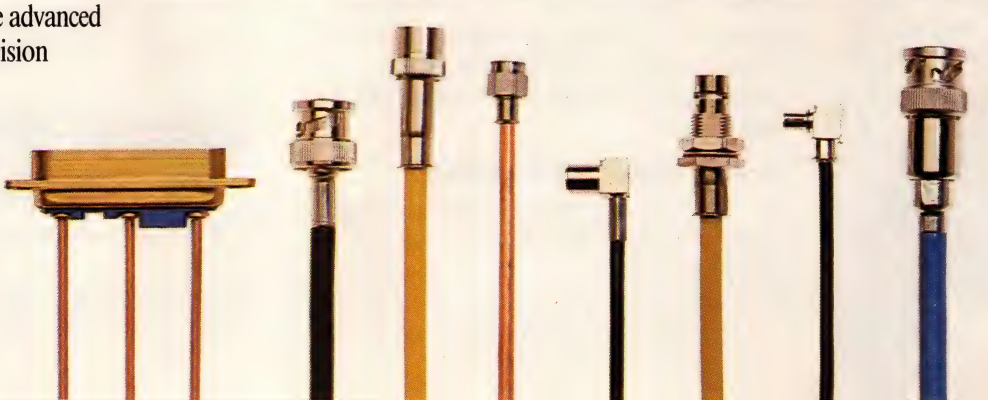
But we would like to remind you of one important event in the world of plotting. We introduced the first wide format laser plotter—the Model 8836. This remarkable machine

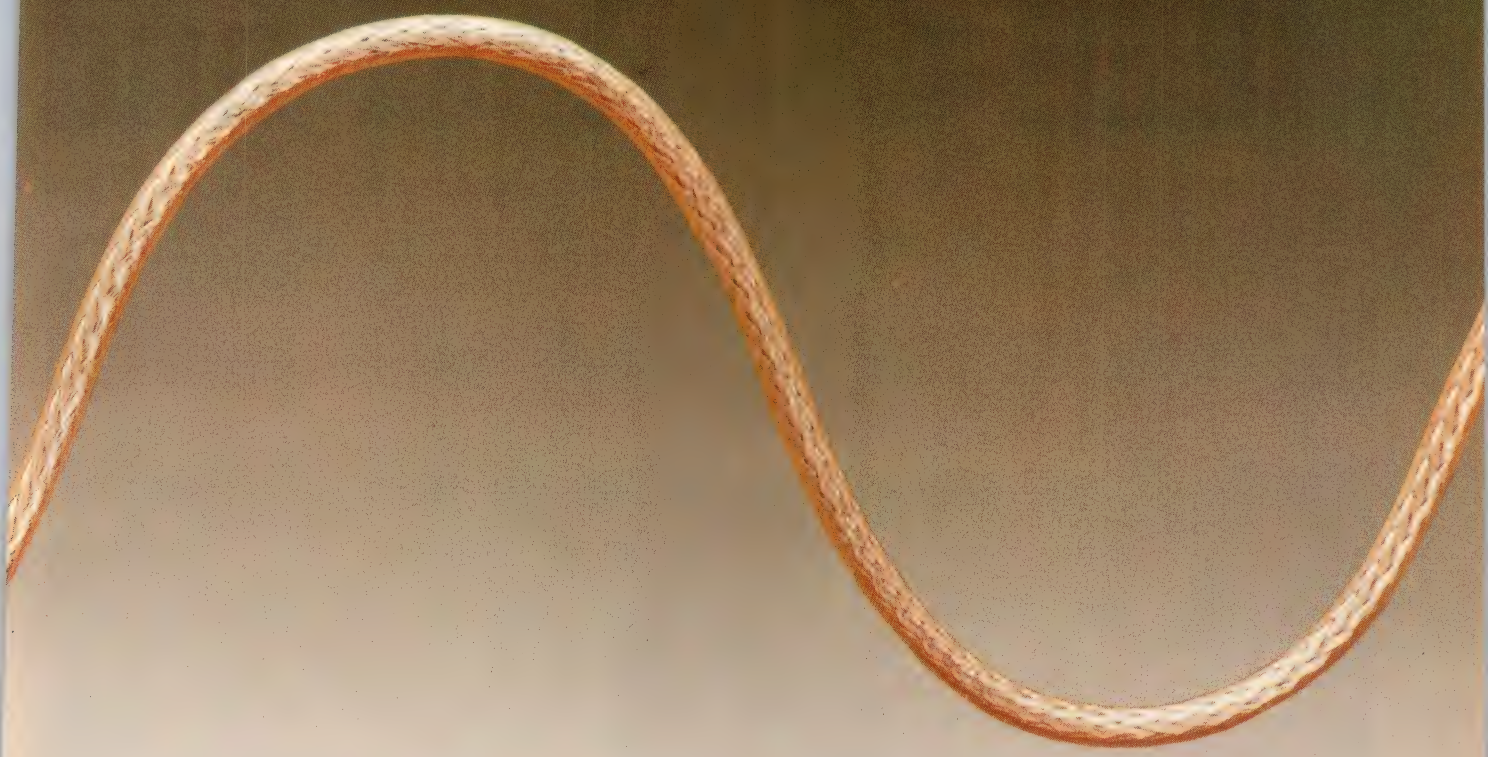




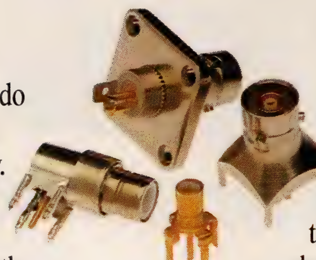








# your sine?



to 26 GHz. And they do it time after time, with unbeatable consistency. All the while saving *you* time—on the line or in the field—with proven crimp/seal technology.

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CIRCLE NO 71

# IEEE-488 test and


***By working with instrument function panels,*** *you can automatically generate programs for test and measurement instruments. (Photo courtesy National Instruments)*

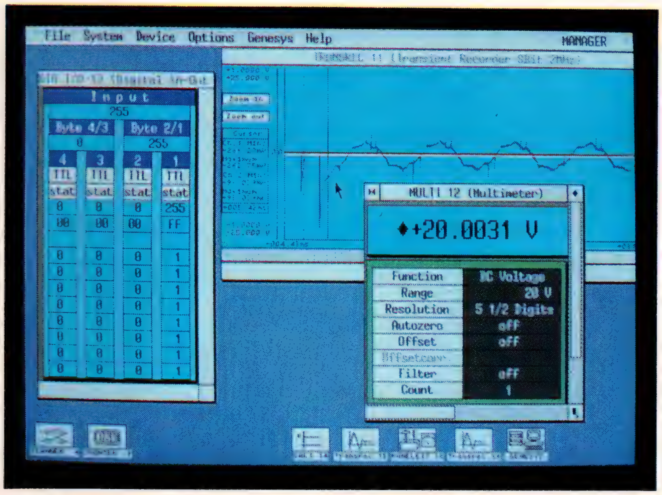
# measurement software

Instrument function panels and automatic code generation are making it easy for the new or infrequent user to write IEEE-488 control programs.

Doug Conner, Regional Editor

Writing IEEE-488 control and data-acquisition programs can be slow work if you use low-level IEEE-488 commands. Most users must study the instrument operating manuals carefully and become fluent in the IEEE-488 low-level instructions for each instrument before writing even the simplest control program. But some software vendors have made life easier by providing software packages with instrument-specific function panels and automatic code generation. Many of these packages also include sophisticated analysis capabilities and graphical presentation of the results.

An instrument function panel is a menu screen that uses simple English commands to set or change instrument controls. These function panels let you program an instrument without learning new commands. If you're familiar enough with an instrument to operate it in its stand-alone mode using the front panel, you should be able to control its operation using an instrument function panel.




***Windowing is a common feature*** *of many IEEE-488 software packages. PCI software from Gould lets you adjust instrument settings while you view outputs.*

**Program instruments in plain English**

Some IEEE-488 software packages offer menu-driven control of instruments, but these menus contain IEEE-488 commands, not plain English commands. For instrument function panels, the IEEE-488 commands have been translated into language that would be obvious to an instrument user, not just an IEEE-488 programmer. For example, the function panels for a

Instrument function panels let you control instruments as easily as you could by using the instrument's front panel.


*Instrument function panels, such as this one from Hewlett-Packard's ITG, let you control instruments using IEEE-488 software as easily as you could by using the instrument's front panel. As you adjust the panel settings, the high-level source code, HP Basic in this case, is automatically generated to form your control program.*

digital storage oscilloscope typically have menus for triggering, timebase, channel settings, and measurements. Within these menus you can set any function that can be set on the digital storage oscilloscope's front panel. A pop-up menu often backs each function and lets you know what your options are. Thus, you don't need to remember the exact wording used for each command.

Instrument function panels also act as checklists to help you make sure that the instrument is in the desired state. You can quickly scan the function panels to see that all settings are correct, just as you would scan the front panel on an oscilloscope to confirm proper instrument settings.

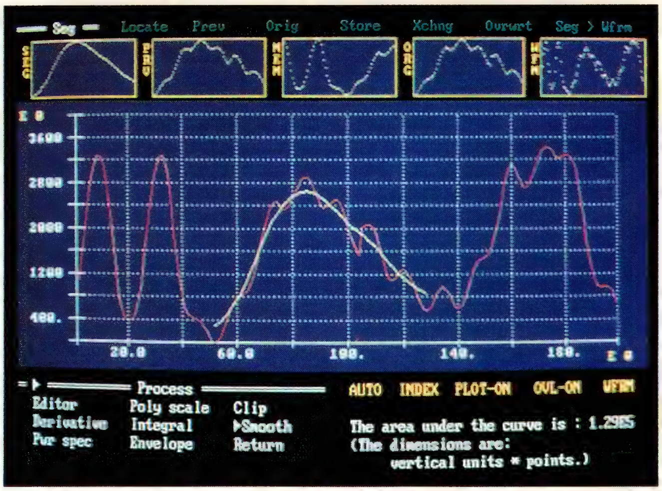
As you change instrument settings on the function panels, you can use an interactive mode for instrument control while you develop your program. As you change function-panel settings, the new settings are sent to the instrument over the IEEE-488 bus. At the same time, a program generator within the software package generates the high-level-language source code to perform these instrument control functions. This high-level-language source code, usually a version of Basic or C, is your IEEE-488 test program.

One attractive feature of function panels and automatic code generation is that you don't have to give up any flexibility in instrument control: You can still use low-level IEEE-488 commands. In most cases, you won't need this flexibility; but it's there when you need to optimize code for speed, debug a hardware problem, or do any other fine tuning.

At least one software package, Interactive Test Generator (ITG) from Hewlett-Packard, tries to keep your automatically generated code fast. ITG uses what HP calls incremental-state programming to avoid wasting time on unnecessary instrument commands. ITG tracks the current instrument state and issues only the commands necessary to reach the next state. Incremental-state programming saves time not only by omitting the transmission of unnecessary commands but also by avoiding the time it takes the hardware to execute those commands.

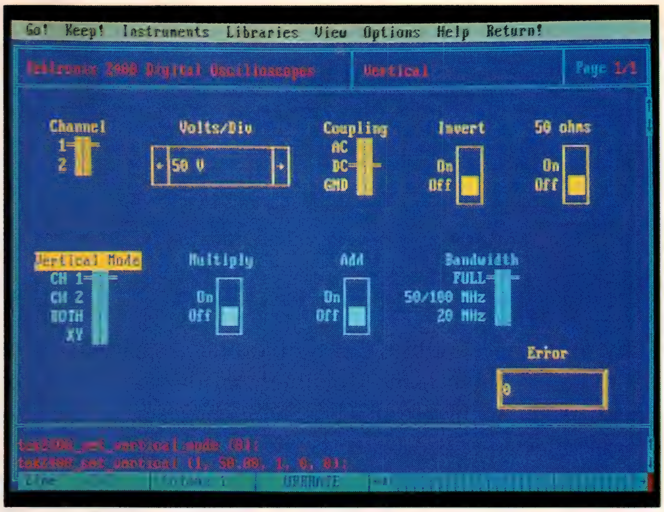
Instrument function panels combined with automatic code generation can help you develop IEEE-488 control programs quickly and easily, especially if you're a novice or an infrequent user. There are, however, some catches.

You'll need a function-panel software driver for each instrument you want to program. These drivers contain instrument-specific menus and the information needed to translate the menu selections into high-level code. Every software product using function panels and automatic code generation offers a library of instrument drivers. None of these libraries is large enough to cover all the instruments you might be using, so the software vendors also provide the information you need to build your own instrument drivers.




*Powerful analysis capabilities are included in many IEEE-488 software packages. By using the waveform processor of Asystant GPIB from Asyst, you can interactively view and analyze waveforms. The five windows at the top keep an ongoing record of the results.*

Writing your own instrument drivers is a time-consuming task. You'll spend lots of time with the instrument's operating manual, but you'll only have to do it once. Some products, such as Wavetek's WaveTest and Gould's Personal Computer Instruments (PCI) software, include dedicated function-panel-generation software. These generators help, but building your own instrument drivers is still time consuming—otherwise software vendors would offer larger instrument libraries.

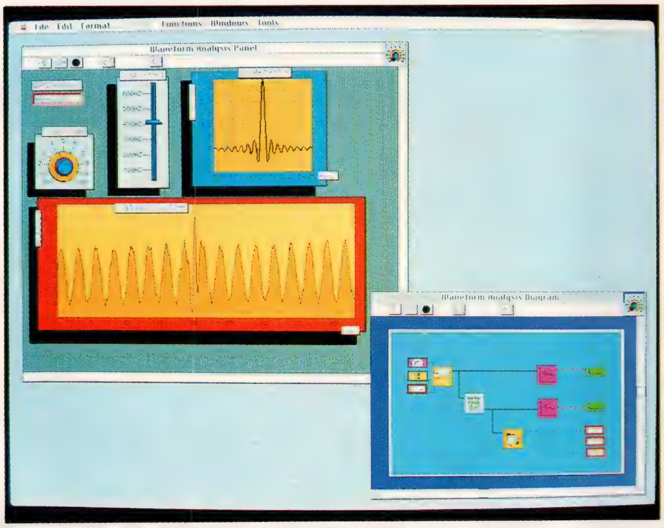



***This instrument function panel*** *is one of several that you can use to control a digital storage oscilloscope. LabWindows from National Instruments automatically generates Basic or C code in the lower window to match your instrument-function-panel settings.*

**Beware of slow windows**

Another potential drawback of function panels and other menu-driven methods of instrument control is that the programming speed might seem slow to the experienced user. Depending on the software and the computer used, changing function panels or windows to access different functions on an instrument can be slow. When it takes more than a few seconds to change function-panel displays, you might wish there were a way to bypass the menus.

Proponents of command-driven software claim that once you've spent some time with the software and hardware—less than you would spend to program your own instrument driver—you could be writing command-driven programs. And you'd be able to do it faster than you could by moving a mouse and waiting for windows to change. Command-driven software might speed up development in cases involving a large number of instruments or instruments with complex setups. But the difficulty of keeping track of all the instrument settings would probably lead you to use function panels or some manual method, if only to keep track of instrument states.



***Virtual instruments*** *are created on the Apple Macintosh using LabView from National Instruments. The lower-right window shows how the blocks are connected to form the virtual instrument. The upper-left window contains the controls for adjusting the input and displays the graphic results. This setup lets you modify settings and immediately see the results.*

Whether instrument control is through function panels or is command driven, frequent or standard setups can often be named and saved. These setups can be recalled and used later, thus saving time and simplifying programming.

Tektronix's EZ-Test III uses another approach for controlling instruments. With EZ-Test III, you set up instrument front panels manually by using an instrument's stand-alone controls. When you have it set up correctly, EZ-Test III queries the instrument for all the settings and stores the actual setup. This method avoids instrument programming issues, at least as far as instrument control is concerned. In order to use EZ-Test III, it must be possible to query an instrument for its state. All of Tektronix's digitizing instruments and many, but not all, instruments from other vendors can be queried.

Instrument control is only one of the tasks you normally need from IEEE-488 software packages. Transferring data, analyzing it, and presenting the results is the complete job.

After you have the instruments set in the desired state, the next step in using IEEE-488 software is data transfer. Some software packages, such as Wavetest and PCI, provide a menu-driven solution with automatic code generation. Other software packages let you write the code in a high-level language to fill or dump arrays of data. Automatic code generation for this step is not critical—especially if you feel comfortable writing code—because this step entails little if any instrument-specific code.

Once you have transferred the data from the instrument into the computer, you typically have access to

Function panels save you from having to learn low-level IEEE-488 commands for instrument control.

any data that would be available on the instrument in stand-alone operation. This information may be all you need if you're using an IEEE-488 setup only for data logging or to speed up tests you could perform manually. But another reason for using IEEE-488 software is to perform analysis beyond the capabilities of the stand-alone instruments.

For example, if one of the instruments you are controlling is a digital oscilloscope, you might have direct access to pulse parameter information like rise time, fall time, pulse width, amplitude, and frequency. But if your digital oscilloscope doesn't support these functions, you can still obtain them by using software packages with analysis capabilities.

Keep in mind, however, that any processing the instrument performs on the data will usually be faster than transferring the data over the IEEE-488 bus to the computer and then using software to analyze the data.

### Use the same software for analysis

**Table 1** lists some of the analysis capabilities found within IEEE-488 software packages. The **table** is only a rough guide for these analytical functions—you'll find quite a bit of variation in the capabilities of different packages in filtering, statistics, curve-fitting, and array operations.

Some of the functions available in analysis packages are convenience functions—routines you could easily write yourself. For example, array operations let you perform mathematical operations on entire arrays without the need to write loops to alter each element

## TABLE 1—REPRESENTATIVE IEEE-488 SOFTWARE PACKAGES

| | | INSTRUMENT CONTROL | | | | | ANALYSIS CAPABILITIES | | | | | | | | | OUT-PUT | | DEBUGGING AIDS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MANUFACTURER | PRODUCT | MENU DRIVEN | COMMAND DRIVEN | FUNCTION PANELS | NUMBER OF INSTRUMENTS IN LIBRARY | AUTOMATIC-CODE-GENERATION LANGUAGE | STANDARD MATH FUNCTIONS | ARRAY MATH | STATISTICS | FFTs AND INVERSES | CONVOLUTION/DECONVOLUTION | FILTERS | CURVE FITTING | INTEGRATION/DIFFERENTIATION | PULSE PARAMETERS | TABULAR | GRAPHICS/PLOTTING | BREAKPOINTS | SOURCE-CODE TRACING | VARIABLE TABLES | IEEE-488 TRAFFIC TRACING |
| ASYST | ASYST 3.0 | | ✓ | | N/A | N/A | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ | | |
| | ASYSTANT GPIB | ✓ | | | N/A | N/A | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| DSP DEVELOPMENT | DADiSP WORKSHEET | | ✓ | | 24 | N/A | ✓ | | ✓ | ✓ | ✓ | ✓ | | ✓ | | ✓ | ✓ | | | | |
| GOULD | PCI | | | ✓ | 25 | BASIC | ✓ | | O | O | | | O | O | | ✓ | ✓ | ✓ | | | |
| HEWLETT-PACKARD | ITG | | | ✓ | 32 | HP BASIC | ✓ | O | O | O | O | O | O | O | O | ✓ | O | ✓ | ✓ | ✓ | ✓ |
| LABORATORY TECHNOLOGIES | NOTEBOOK GPIB | | ✓ | | | N/A | ✓ | | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | ✓ | | | | |
| NATIONAL INSTRUMENTS | LABWINDOWS | | | ✓ | 55 | BASIC, C | ✓ | ✓ | ✓ | O | O | O | O | O | O | ✓ | ✓ | ✓ | ✓ | ✓ | |
| | LABVIEW | | | ✓ | 100 | G | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | |
| | MEASURE | | ✓ | | N/A | N/A | ✓ | ✓ | ✓ | | | | | | | ✓ | ✓ | | | | |
| PHILIPS/FLUKE | TEST TEAM | | | ✓ | 25 | BASIC, C | ✓ | ✓ | ✓ | O | O | O | O | O | O | ✓ | ✓ | ✓ | ✓ | ✓ | |
| SUMMATION | TEST WINDOWS 3.1 | | | ✓ | 200 | TEST BASIC | ✓ | | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| TEKTRONIX | E2-TEST III | ✓ | | | N/A | N/A | ✓ | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| | GURU II | | ✓ | | N/A | N/A | ✓ | | | | | | | | ✓ | ✓ | | | | | ✓ |
| WAVETEK | WAVETEST 2.5 | | | ✓ | 75 | BASIC | ✓ | | | | | | | | | ✓ | | ✓ | ✓ | ✓ | ✓ |

✓=FEATURE O=OPTION N/A=NOT APPLICABLE

in the array. Other functions, such as curve fitting and filtering, are more complex, and writing them would be a major programming exercise for most users.

Of course, you can take the data acquired by any IEEE-488 software package, write it to a file, and use another software package to perform analysis on the data. But having the analysis capability in the same package as your control and data-acquisition capabilities means one less package to learn and can also save you time.

If the software package operates as a virtual instrument, such as National Instruments' LabView, data can be taken, analyzed, and presented in one continuous process. A virtual instrument is an instrument created in software although it requires a real instrument to take the raw data. For example, the voltage-vs-time data taken by a digital oscilloscope can be processed in software to give you the results of a virtual spectrum analyzer. If you're using separate software packages, you're usually forced to operate in a batch-process mode. In this mode, the IEEE-488 software acquires and stores the data, and then a separate analysis package processes it.

| COMPUTERS SUPPORTED | PRICE | NOTES |
|---|---|---|
| IBM PC/XT/AT, IBM PS/2 | $2095 | |
| IBM PC/XT/AT, IBM PS/2 | $695 | |
| IBM PC/XT/AT, DEC, HP, SUN, MASSCOMP | $795–$4995 | |
| IBM PC/XT/AT | $5395–$9595 | $9595 INCLUDES ALL OPTIONS |
| HP 9000 SERIES 200/300, HP VECTRA, IBM PC/AT | $1490 | WORKSTATION IS REQUIRED FOR FUNCTION PANELS |
| IBM PC/XT/AT, APPLE MAC | $995 | |
| IBM PC/XT/AT | $495 | |
| APPLE MACINTOSH | $1995 | |
| IBM PC/XT/AT | $495 | REQUIRES LOTUS 1-2-3 OR LOTUS SYMPHONY |
| IBM PC/XT/AT | $1515 | |
| IBM PC/AT | $3300 | |
| IBM PC/AT | $1795 | |
| IBM PC/XT/AT | $495 | |
| IBM PC/AT | $3990 | |

## Integrated analysis is more efficient

Batch processing of data is often acceptable in standardized test applications. In these cases, you may just be recording the results of tests and, perhaps, some test statistics. However, in any type of testing or design where the action you perform next depends on the results of the previous tests, you'll often save time by using an IEEE-488 software package with integrated analysis functions.

For example, in a design situation, you may need to design a filter circuit to remove some uncharacterized noise from a waveform. Digitizing the waveform, examining the power spectrum of the noise, and developing a suitable filter in software before designing the filter circuit might help you design the right circuit without trial and error. Performing all these functions with one software package will save you time.

## Don't forget about presentation of results

A well-integrated software package doesn't stop at analysis; it also provides for the flexible presentation of the results. You'll find lots of variation in the data-presentation capabilities of software packages. Some packages have virtually no such capabilities and assume that you'll be using another software package. Packages that do provide plotting vary in their sophistication. Some provide autoscaling, labels, and logarithmic plots with user variables such as color, data-point identifiers, and line type. Others are more limited.

IEEE-488 software packages also differ in their software-debugging capabilities; it's important to consider your needs for the type of software you're using. If you're programming primarily or exclusively in a high-level language, there are lots of opportunities for programming errors to creep in. In this case, it's a good idea to have plenty of debugging capabilities in the software.

If you're using menus and automatically generated code, you're less likely to need sophisticated debugging capabilities. But unless your programs are short and simple, it's helpful to have some way to set break-

As you adjust instrument-function-panel settings, the software automatically generates high-level source code to form your control program.

points, single step, or perform source-code tracing. With these capabilities, you can make sure that the program is doing what you want it to.

Some of the IEEE-488 software packages include features not mentioned in **Table 1.** For example, WaveTest lets you write programs using either function blocks in what Wavetek calls the icon window or flow charts in the flow-chart window. You can develop your program using either method, and the software will automatically generate your program using the other method. The software also keeps both programs up to date as you make changes and automatically generates the test program in Basic.

One benefit of this method is that your program is automatically documented with a flow chart that stays current as you make program changes. By using WaveTest's menus, you can completely develop a Basic test program without writing one line of Basic code. But if the need arises, you can write part or all of the test program directly in Basic.

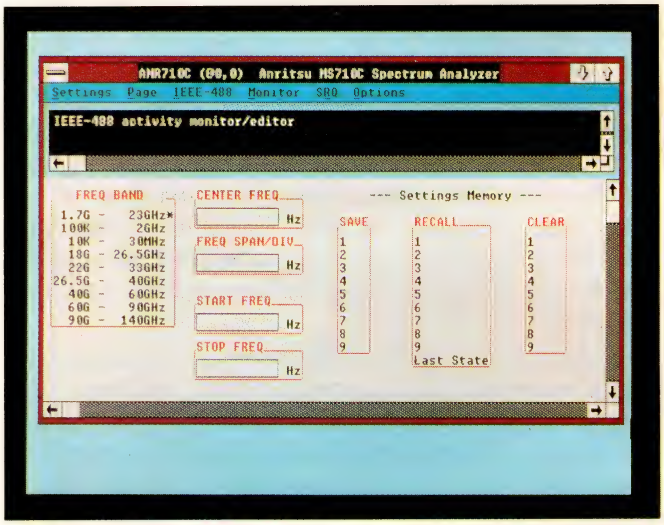
WaveTest has no analysis capabilities other than the math functions available in Basic. If you need more advanced analytical capabilities or graphics output, you'll need to pass the data files to other software packages.

PCI also offers complete function panels or menus and automatic code generation in Basic for all phases of program development. You can perform instrument control, data acquisition, analysis, and graphical presentation. An optional analysis package integrates cleanly into the basic package. Although it's not the most complete analysis package available, it's adequate for many applications.

A software package with excellent analytical capabilities is Asyst 3.0 from Asyst Technologies. This software product offers integrated data acquisition, analysis, and graphical presentation. Asyst 3.0 is command driven rather than menu driven, and you can use it to build custom commands, menus, and application programs.

Asystant GPIB, another product from Asyst Technologies, is a menu-driven software package for IEEE-488 use. Although menu-driven, the menus are not function panels but menus of IEEE-488 commands. Asystant GPIB also has good analytical capabilities.

Another software package with excellent analytical capabilities is the DADiSP worksheet from DSP Development Corp. DADiSP is an integrated data-acquisition, analysis, and graphical-presentation software product. This command-driven software package offers




***Instrument function panels,*** *such as this one from Summation's TestWindows, let you save and recall commonly used setups.*

an instrument-command library, but not in the form of function panels.

LabWindows from National Instruments offers instrument function panels and automatic code generation. Although you'll have to write some high-level-language code for your test programs, you shouldn't have to write any low-level IEEE-488 control commands. You can write code in either Microsoft QuickBasic or Microsoft C.

At $495, LabWindows is the least expensive package offering instrument function panels, automatic code generation, some analytical capabilities, and a graphics library for screen output and plotting. Add the optional advanced analysis package at $895, and you get powerful analysis capabilities. LabWindows also provides an excellent set of debugging tools, such as breakpoints, source-code level tracing, and variable displays that show the contents of all currently defined variables.

The LabView software package, another product from National Instruments, is based on the idea of building virtual instruments to process data. As you develop programs, you build your own library of virtual instruments that you can use for future applications. LabView uses its own programming language called "G." You can write an application program by graphically connecting virtual instruments that act on the data. This graphical representation of connected instruments also documents what the program does, at least at the top level.

Measure is yet another IEEE-488 software product from National Instruments. Measure is designed for

## Manufacturers of IEEE-488 software packages

For more information on IEEE-488 test and measurement software packages, such as those described in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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FAX 617-494-1394
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those who want to use Lotus 1-2-3 or Lotus Symphony for data analysis.

Test engineers don't often use IEEE-488 software to make sets of routine measurements when evaluating electronic designs and products. One reason is that many engineers think they would spend more time learning the software and writing the program than they would taking the data manually. Instrument function panels and automatic code generation are changing this perception. And if you need to perform additional analysis on data after acquiring it, you have even more reason to consider using IEEE-488 software to automate your work. EDN

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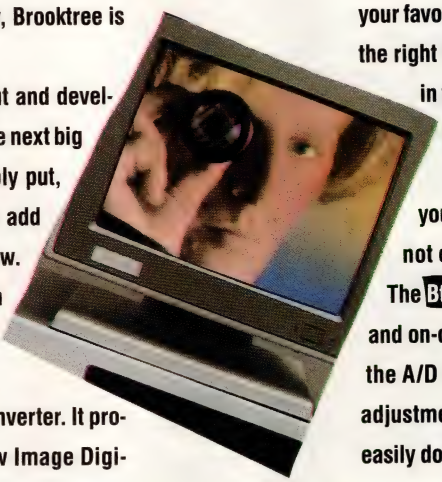

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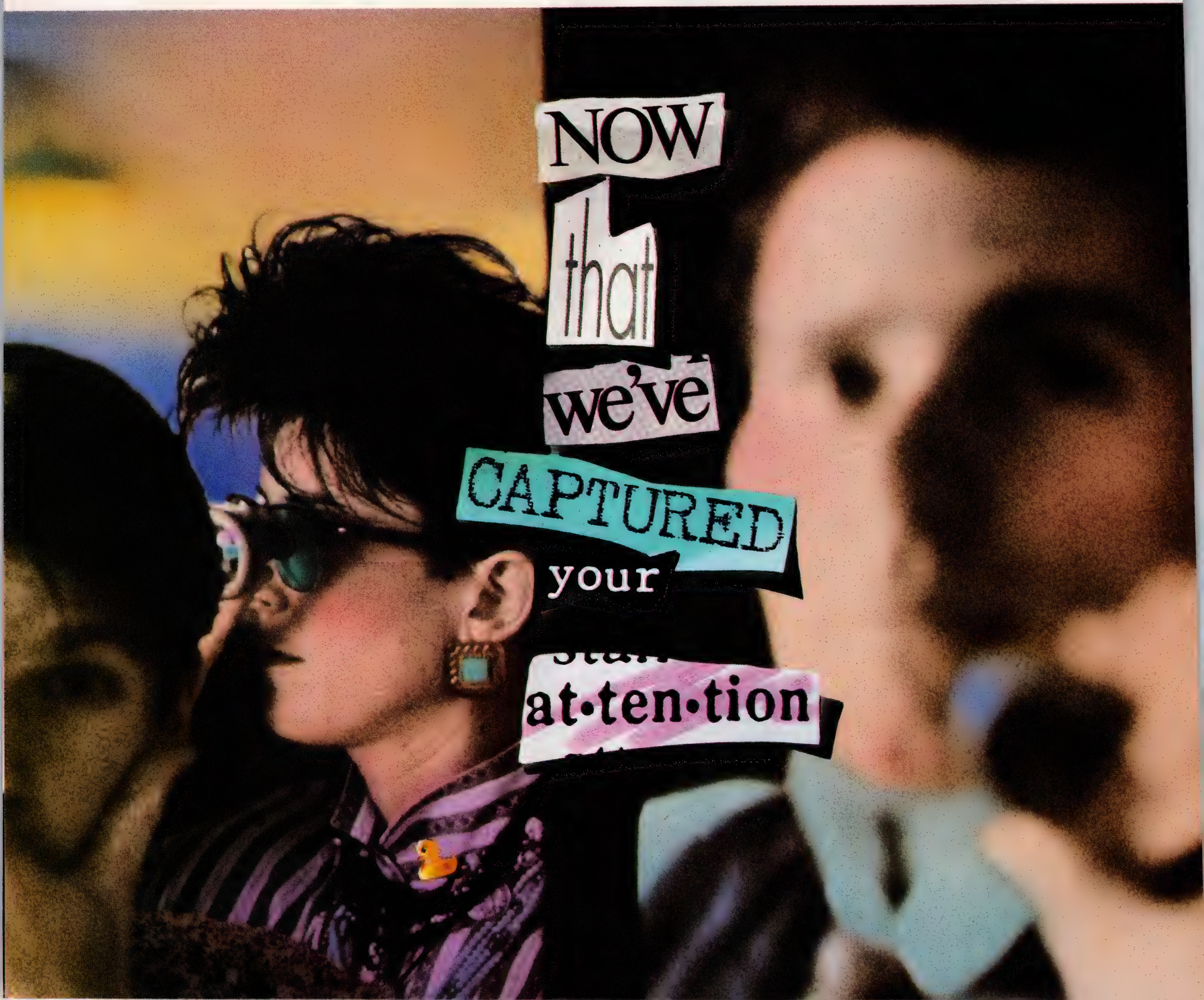

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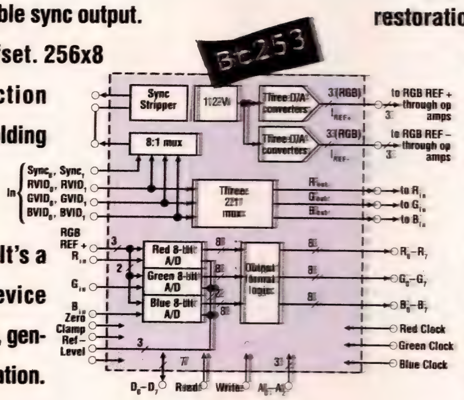


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DESIGNER'S GUIDE

dynamic RAMs
Part 2

# Tailor memory-system architecture for your chosen DRAM

*To tap the full potential of a dynamic RAM (DRAM), you must tailor your memory-system architecture for the DRAM you've chosen. This article, part 2 of a 4-part series, examines your architectural options in designing a memory system. Part 1 reviewed the fundamentals of DRAMs and how to choose them; parts 3 and 4 will focus on DRAM controllers and DRAM-board layout.*

Ronald Wawrzynek, *Texas Instruments*

When you design a dynamic-RAM (DRAM) system, you must choose its architecture carefully. The architecture affects the system's memory-access speed, cost, and power consumption, and it may influence your selection of a DRAM. In creating the system, you can choose from a number of architectural options, each involving certain tradeoffs. To come up with the optimal architecture for your application, examine the options and their concomitant tradeoffs carefully before making your choice.

First, however, it's useful to know a little about how DRAM systems are organized. Because most µPs manipulate bytes, it's convenient to arrange a DRAM system as byte-wide blocks. You can easily accomplish this memory structure by accessing eight $N \times 1$-bit DRAMs in parallel. Microprocessors that operate on multiple-byte units—such as 16- and 32-bit µPs—access data by addressing either multiple blocks or multiple rows within a block.

Because today's µPs can access more than the N locations indigenous to today's $N \times 1$ DRAMs, designers typically build large memory structures in sections, or "banks." A memory bank is usually as wide as the CPU's data path and as long as the DRAM's capacity (N). For example, memory systems with 8-bit µPs are built with $N \times 8$-bit banks, and systems with 32-bit µPs use $N \times 32$-bit banks. However, the most convenient structure for a 16-bit µP with an 8-bit data path, such as the 8088 CPU, is one with $N \times 8$-bit banks.

All of the DRAMs within a bank have a common Row Address Strobe signal, which the DRAM controller supplies via the $\overline{\text{RAS}}$ line. Essentially, the DRAM controller uses the $\overline{\text{RAS}}$ line as a bank-select signal. Most DRAM controllers include four independent RAS output drivers for driving four separate memory banks.

There are occasions when the system's CPU desires access to selected bytes within a memory bank. For example, a 32-bit µP may need 16-bit data for an internal array computation. Because the bytes may not lie on a 32-bit boundary, the CPU must be able to select each byte individually. You can configure the DRAM controller to access a byte by issuing either separate $\overline{\text{CAS}}$ or separate $\overline{\text{WRITE}}$ lines to the individual blocks within a bank **(Fig 1)**. Whether you use a separate $\overline{\text{CAS}}$ or a separate $\overline{\text{WRITE}}$ line often depends on the access mode available for the DRAM.

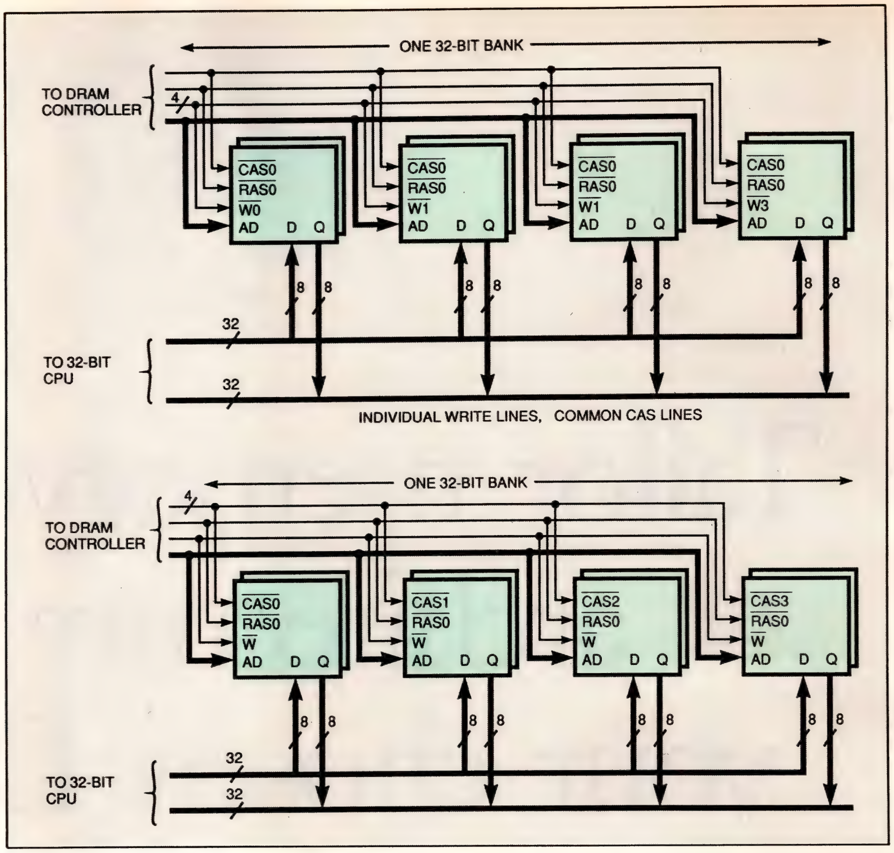


*Fig 1—**The two most common methods for accessing data** in a memory bank with multiple bytes is either to use a common CAS line and separate WRITE lines for each block **(a)**, or to use a common WRITE line and separate CAS lines for each block **(b)**.*

DRAM architectures fall into two basic groups: the byte-oriented-CAS and the bank-oriented-CAS arrangements. **Figs 2** through 8 illustrate some of your architectural options for constructing a DRAM system with these two arrangements. (Note that the figures don't show all of the control signal lines; they show only the lines necessary to exemplify the different ways of interfacing some popular CPU families to DRAMs.)

The byte-oriented-CAS arrangement, shown in **Fig 2**, interfaces an Intel 16-bit 8086 µP to a 512k-byte memory bank. Because the µP has a 16-bit data path, the memory bank is organized as two 256k-byte blocks labeled "even" and "odd." The even block stores the lower byte ($D_0$ to $D_7$) and the odd block stores the upper byte ($D_8$ to $D_{15}$) of a 16-bit data word. The DRAM controller has two independent $\overline{CAS}$ lines for accessing either the even or the odd byte. The µP accesses the even block (or byte) on even address boundaries (1, 2, 4, . . . ) and the odd block (or byte) on odd address boundaries (1, 3, 5, . . . ).

The DRAM controller uses the $A_0$ line and the $\overline{BHE}$ (Byte High Enable) line from the µP to decide whether to transfer a high byte, a low byte, or the entire 16-bit word. Address lines $A_1$ to $A_{18}$ provide the 18 addresses required to access the 256k-byte memory space. The controller must internally generate the separate row

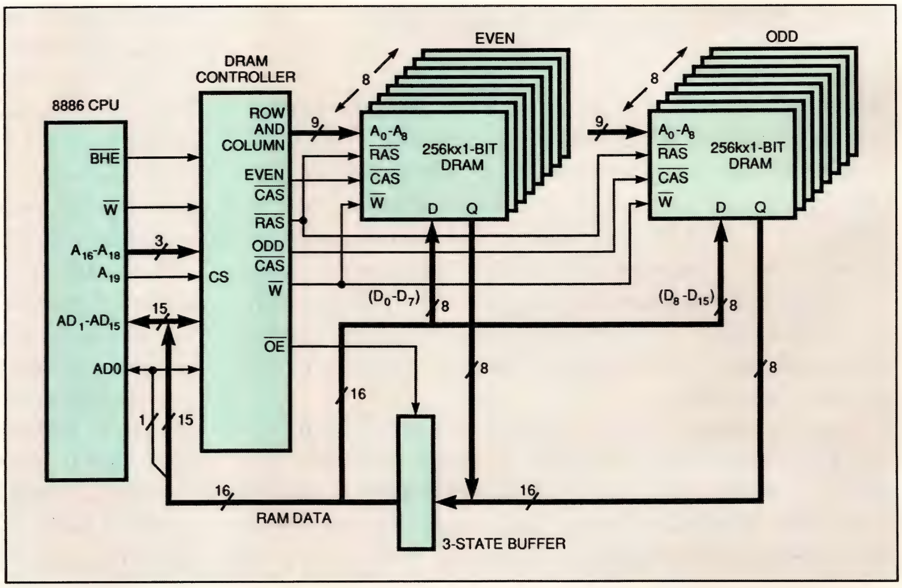


*Fig 2—**The byte-oriented-CAS arrangement employs** separate $\overline{CAS}$ lines for each byte in a memory bank and a common $\overline{WRITE}$ line. Because the 8086 µP has a multiplexed address and data bus, an external 3-state buffer is necessary to prevent bus conflicts.*

*In the bank-oriented-CAS arrangement, the two blocks in a 16-bit bank have a common $\overline{CAS}$ line, but independent $\overline{WRITE}$ lines.*

and column addresses for each block. Because the 8086 μP has a 16-bit multiplexed address/bus, the upper four address lines ($A_{16}$ to $A_{19}$) are address-only lines and are shown separately in the diagram. The lower 16 address lines ($A_0$ to $A_{15}$) must connect to a 3-state buffer, which implements a bidirectional data bus. When the CPU is ready to read data, and valid data is available at the DRAM's Q outputs, the DRAM controller issues an enable signal ($\overline{OE}$) to the 3-state buffer.

Both blocks in the memory bank share the same $\overline{RAS}$ and $\overline{WRITE}$ lines. During a write cycle, the controller issues a $\overline{RAS}$ and a $\overline{WRITE}$ command to both blocks. However, it issues a $\overline{CAS}$ command only to the even or the odd block when writing a byte. When writing a word, it issues the $\overline{CAS}$ command to both blocks. The DRAM controller uses the μP's $A_{19}$ address line as a chip-select line. By connecting the inverted $A_{19}$ address line to the chip-select pin on an identical DRAM controller that's supervising another 512k-byte bank, you can expand the memory capacity to the 1M-byte address limit of the 8086 μP.

### CPU's construction affects memory design

The byte-oriented-CAS arrangement for interfacing a Motorola 16-bit 68000 μP to a 512k-byte DRAM bank would be slightly different (**Fig 3**). The memory bank is still grouped into two 256k-byte blocks (labeled "upper" and "lower"), because the 68000 also has a 16-bit data path. However, the 68000 doesn't have an $A_0$ address line for selecting the upper or lower block. Instead, the μP decodes the $A_0$ address internally and generates an upper data signal ($\overline{UDS}$) and a lower data signal ($\overline{LDS}$), which the DRAM controller uses for byte selection. In addition, the 68000 incorporates separate address and data lines.

In this system, as in the 8086 memory system, the DRAM controller generates separate $\overline{CAS}$ lines for each block and common $\overline{RAS}$ and $\overline{WRITE}$ lines. The DRAM controller uses address lines $A_1$ to $A_{18}$ from the CPU to generate the row and column addresses for each block. Because the 68000 has a 16M-byte address limit, the design connects address lines $A_{19}$ to $A_{23}$ to a 1-of-32 decoder for generating 32 chip-select lines. In this manner, you can expand the memory in 512k-byte increments by duplicating the DRAM bank and controller and connecting the chip-select pin for each controller to one of the 32 decoder-output lines.

The 3-state buffer shown in the diagram is necessary only when you employ a delayed-write cycle. As Part 1 of this article (EDN, March 30, 1989, pg 155) explains, the delayed-write cycle briefly enables the DRAM's output buffers, which can cause a bus conflict unless there's an external buffer. The external buffer is not necessary when you employ an early-write cycle, so you can connect the DRAM's D and Q pins, thus effecting a bidirectional data bus.

You can also interface the system CPU to the DRAM by using a bank-oriented-CAS architecture. **Fig 4** shows a 68000 CPU that communicates with two mem-

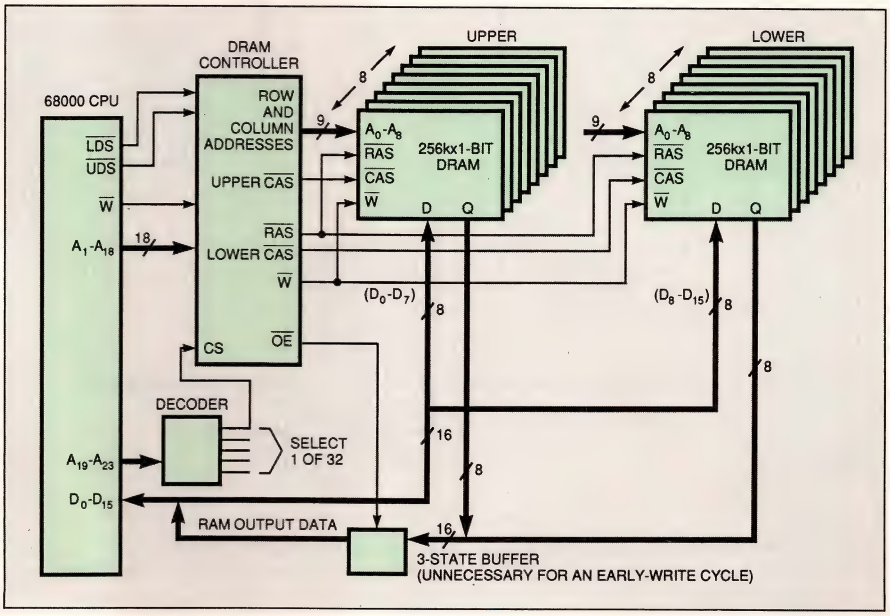


***Fig 3—The byte-oriented-CAS arrangement for the 68000** CPU differs slightly from the arrangement for the 8086 μP. Because the 68000 μP has a separate address and data bus, you require an external 3-state buffer only when employing a delayed-write cycle.*

*A memory bank is usually as wide as the CPU's data path and as long as the DRAM's capacity.*

ory banks. In this arrangement, a single DRAM controller generates separate $\overline{CAS}$ and $\overline{RAS}$ lines for each bank. Both of the control lines are common to both bytes in each bank. In the bank-oriented-CAS architecture, unlike the byte-oriented-CAS scheme, the lower bytes and the upper bytes of the two banks share respective $\overline{WRITE}$ signals.

The bank-oriented-CAS arrangement requires a bidirectional buffer that has two byte-enable control lines and resides in the data path between the CPU and the system memory. Because the CPU is capable of writing byte-wide data, the DRAM controller must separately enable each byte in the bidirectional buffer. Without separate enable lines, it is possible to incur bus conflicts when writing a byte to memory, because the output buffers for the alternate block turn on when the controller drives the common $\overline{RAS}$ and $\overline{CAS}$ lines low.

Both the byte-oriented-CAS and the bank-oriented-CAS arrangements can be employed in a variety of ways. For example, many high-speed memory systems use a bank-interleave architecture to eliminate CPU wait states. This concept organizes successive memory locations into different memory banks. When the CPU reads data from successive locations, the controller accesses the next bank while the DRAMs in the previously accessed bank execute a precharge operation. Because this architecture effectively makes the precharge period transparent, the ta(R) (the delay time after the falling edge of the $\overline{RAS}$ line and before valid data appears at the DRAM output) determines the read cycle time. However, successive reads from the same memory bank must wait for the precharge period to elapse before the controller can access the bank.

**Fig 5** illustrates a bank-interleave structure that interfaces four 512k-byte memory banks to a 68000 CPU by using a bank-oriented-CAS arrangement. The controller selects one of the banks by decoding the CPU's $A_1$ and $A_2$ address lines. The CPU's address lines $A_3$ through $A_{20}$ identify the individual locations within each block of memory. During a read operation, the DRAM controller keeps a record of the bank that's currently being accessed in order to compare it with

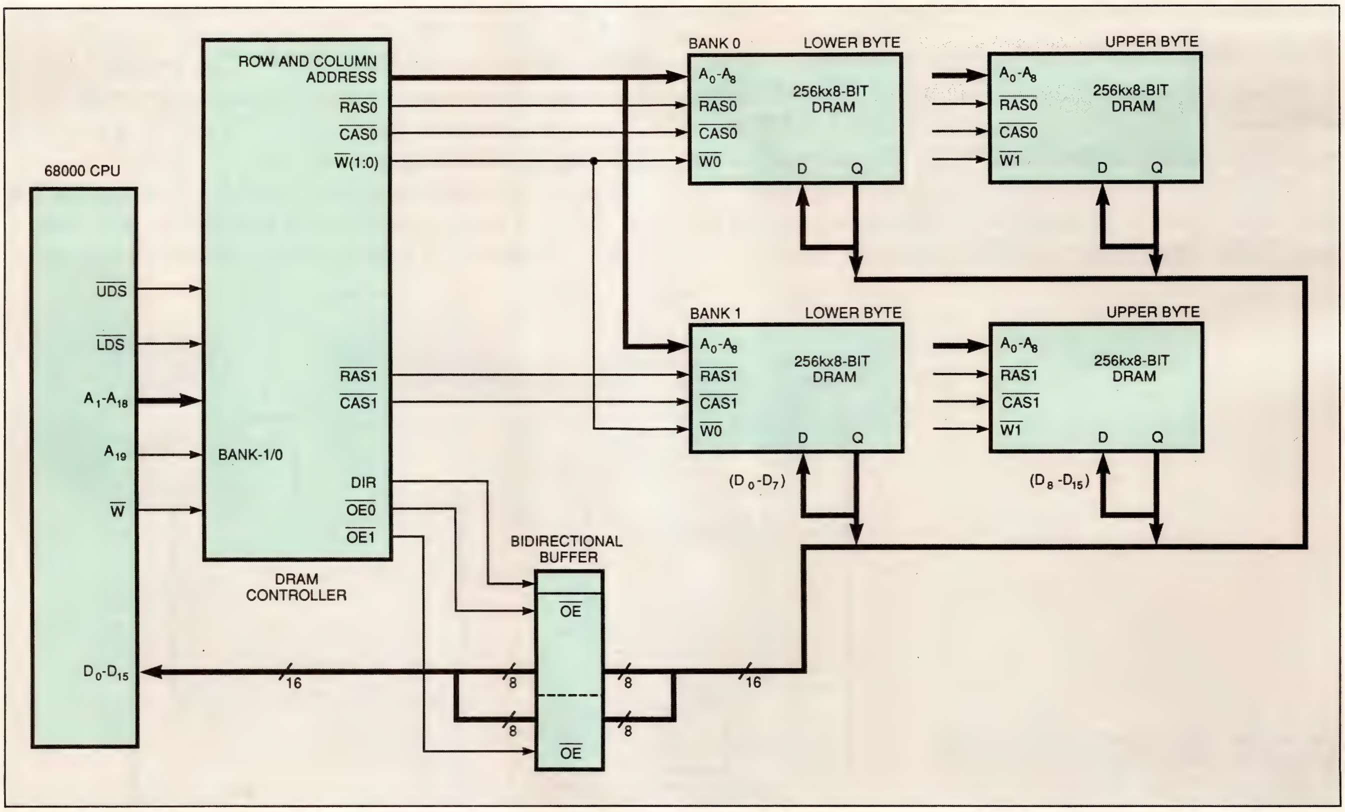


***Fig 4—In the bank-oriented-CAS arrangement,** each bank has a common $\overline{CAS}$ line, but a separate $\overline{WRITE}$ line for each byte within the bank. Because the arrangement must be able to access individual bytes, the DRAM controller must separately enable each byte in a bidirectional buffer.*

the next bank request. If successive bank requests are the same, the DRAM controller must wait for the precharge period to elapse before initiating the next read cycle.

Because a μP generally accesses successive locations in memory when executing a program, the average read-access time for a memory with a bank-interleave structure is typically ta(R) seconds. DRAMs' ta(R) specifications typically range between 100 and 250 nsec, although 80-nsec DRAMs are available.

**Fig 6** shows a byte-oriented-CAS arrangement for an interleaved memory architecture. What differentiates this arrangement from the bank-oriented-CAS scheme is the way in which the $\overline{\text{CAS}}$ and $\overline{\text{WRITE}}$ lines are interconnected. In the byte-oriented-CAS arrangement, one $\overline{\text{WRITE}}$ line is common to all of the blocks. Two $\overline{\text{CAS}}$ lines enable either the lower or the upper block of memory. The interleaved memory architecture is ineffective for DRAMs with cyclic access modes such as nibble mode, byte mode, and serial mode. Such DRAMs access sequential locations that are internal to the DRAMs, a scheme that defeats the purpose of interleaved memory banks.

### Static-column-access mode is fast

The static-column-access mode not only assumes that the CPU accesses data sequentially but also that it accesses data within one row most of the time. The static-column architecture is a nonoverlapping structure in which the lower and upper boundaries of successive banks are adjacent. The memory is organized in a bank-oriented-CAS arrangement, which enables the mode to cross boundaries when accessing columns for a particular row address.

To initiate a static-column read-access cycle, the controller drives the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines low. If the controller detects that the next read is from the same row, it maintains a low on the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines and

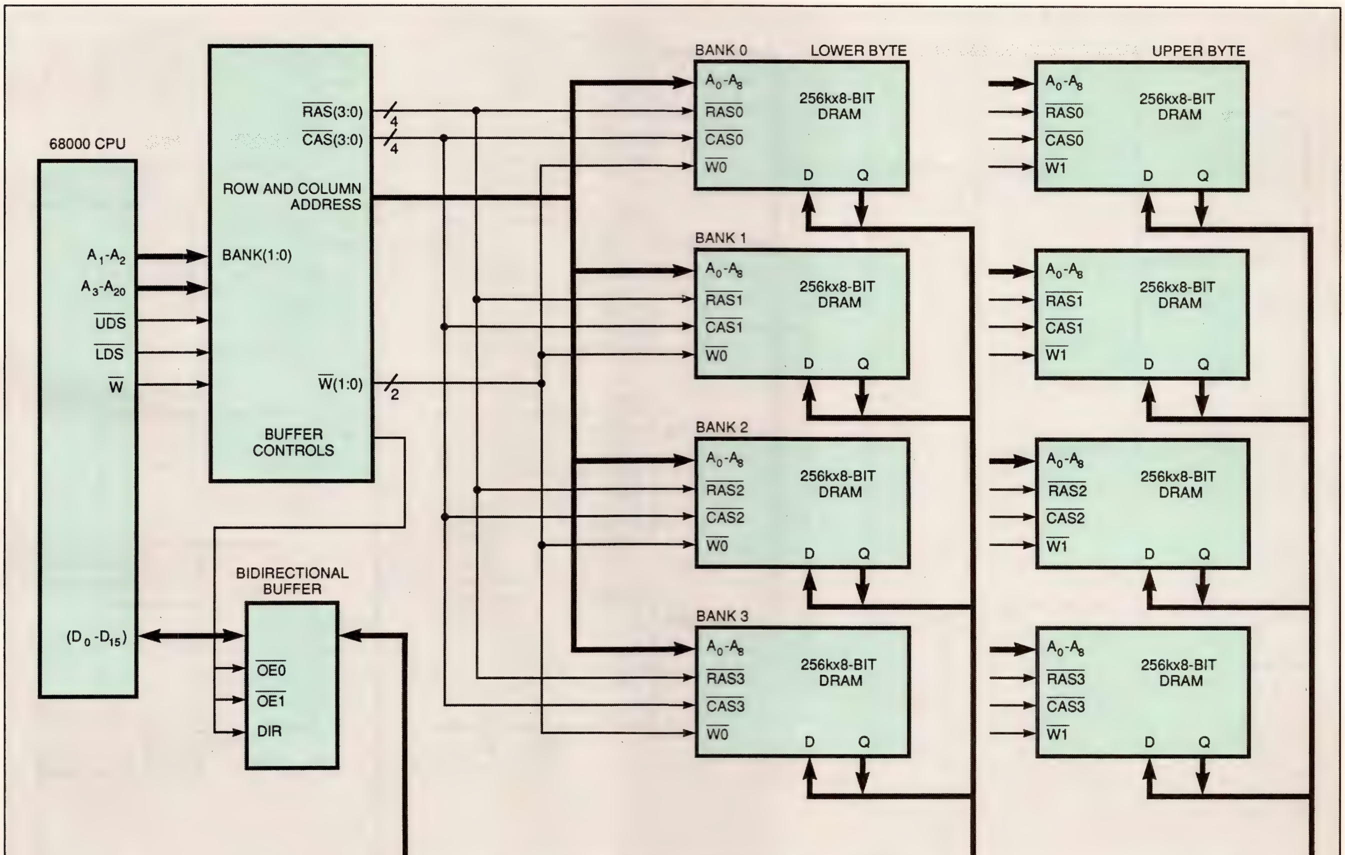


***Fig 5—Interleaving four memory banks*** *in a bank-oriented-CAS arrangement requires a controller with four independent $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ lines, each driving separate banks. In addition, the controller needs two $\overline{\text{WRITE}}$ lines—one for the lower byte and one for the upper byte.*

*The DRAM controller uses the $\overline{RAS}$ line as a bank-select signal.*

issues the next column address. This operation eliminates the delays that the $\overline{CAS}$ line and the precharge time incur. If the next memory read is not from the same row, the controller must return both the $\overline{RAS}$ line and the $\overline{CAS}$ line high before beginning a new read cycle.

**Fig 7** shows a 2-bank memory system employing a static-column architecture. The DRAM controller uses the $\overline{UDS}$ and $\overline{LDS}$ signals from the 68000 µP to select distinct bytes within a bank. In addition, address lines $A_1$ through $A_{18}$ select the individual locations within the block, and address $A_{19}$ functions as a bank-select line.

The static-column mode not only requires separate $\overline{WRITE}$ lines for each byte within a bank, but also requires that the $\overline{WRITE}$ lines for each bank be independent. The DRAM controller, shown in **Fig 7**, directs the two $\overline{WRITE}$ lines to either Bank 0 or Bank 1 by using the bank-enable lines ($\overline{BANK0}$ or $\overline{BANK1}$) to control an external multiplexer.

When the CPU is crossing bank boundaries to access data, it's possible for the $\overline{CAS}$ lines for both banks to remain low during static-column access. In this case, the DRAM output drivers for each bank are continuously enabled, so external 3-state buffers are necessary. To prevent bus crashes, the controller enables only the external buffer for the currently accessed bank by using the $\overline{BANK0}$ and $\overline{BANK1}$ lines.

Page-mode access is similar to static-column-mode access except that the controller returns the $\overline{CAS}$ line high after each data transfer. Therefore, you can incorporate the bank-oriented-CAS architecture shown in **Fig 7** in a page-mode design without the output 3-state buffers.

In sum, you must decide early in the design cycle whether to use a byte-oriented-CAS or a bank-

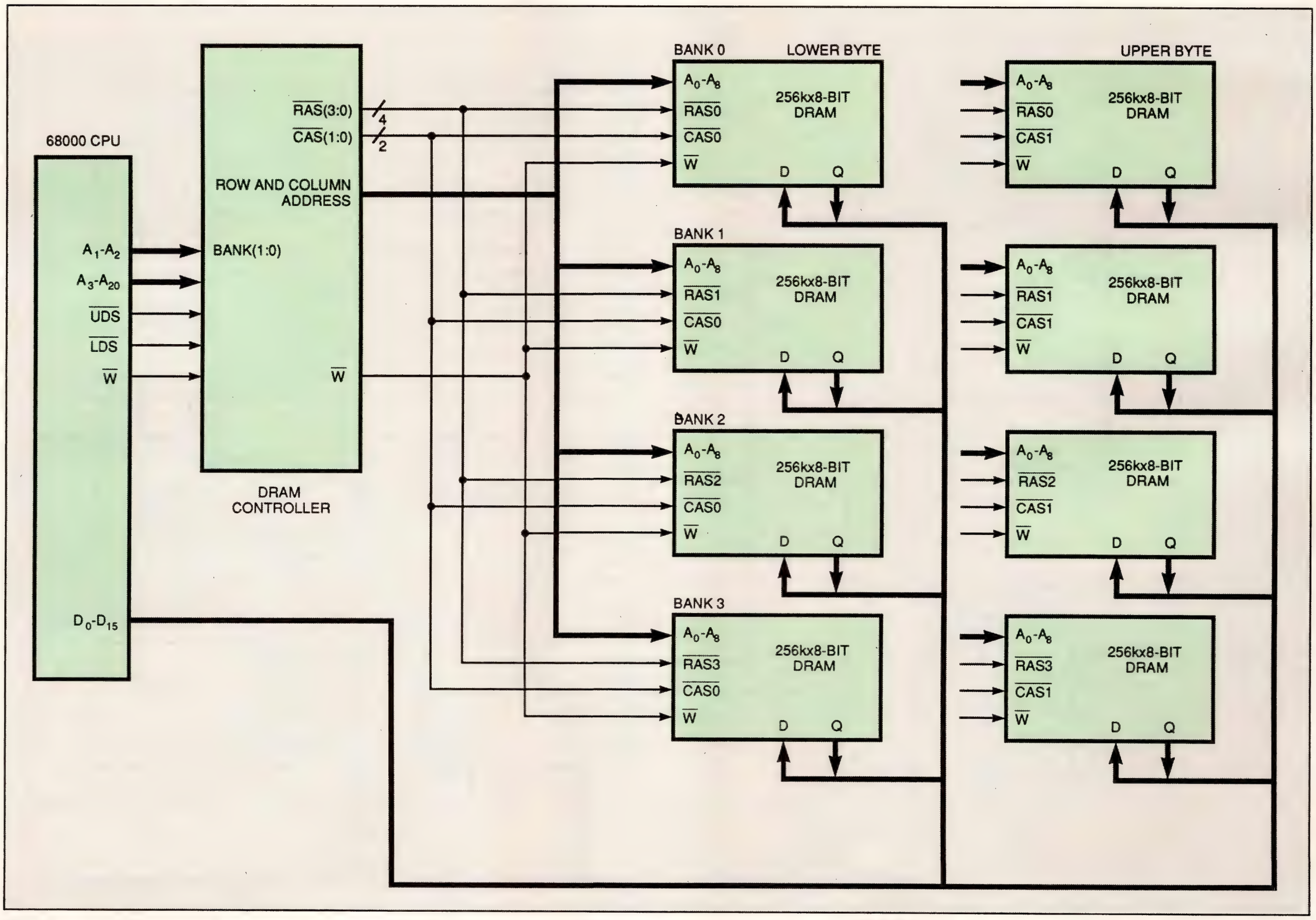


***Fig 6—An interleaved memory*** *connected in a byte-oriented-CAS arrangement requires a $\overline{RAS}$ line for each bank in the memory system. The controller accesses the lower and upper bytes with separate $\overline{CAS}$ lines, but uses a common $\overline{WRITE}$ line.*

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*In the byte-oriented-CAS arrangement, the two blocks in a 16-bit bank have a common $\overline{\text{WRITE}}$ line but independent $\overline{\text{CAS}}$ lines.*

oriented-CAS arrangement. Your decision will be influenced by the type of DRAM the design employs as well as by the complexity of the DRAM-support circuitry.

The byte-oriented-CAS arrangement is perhaps the most popular, because it generally requires less support circuitry, such as external 3-state buffers. In addition, the arrangement lets you easily implement RAS-only refresh, the most common refresh method. However, the byte-oriented-CAS defers to the bank-oriented-CAS arrangement for systems that use other refresh methods or advanced access modes such as static-column-mode access. Static-column-mode DRAMs virtually require a bank-oriented-CAS arrangement. To take advantage of these DRAMs' fast access times, you must have the entire memory bank turned on and waiting for the next column address.

Generally, your choice of whether to use a byte-oriented-CAS scheme or a bank-oriented-CAS arrangement will happen by default; it'll follow naturally from your choice of a refresh method and an access mode for your system. Once you've made those choices, the orientation you'll prefer for the $\overline{\text{CAS}}$ line will usually be obvious. EDN

## Author's biography

*Ronald Wawrzynek is a project engineer for a DRAM-controller ASIC design at Texas Instruments' Information Systems and Services Div (Richardson, TX). He has been at TI for three years, and he previously held a co-op position at IBM (Boca Raton, FL). Ron obtained a BS in electrical and computer engineering from Clarkson University, and is a member of the IEEE. He enjoys golf, cycling, and skiing in his spare time.*

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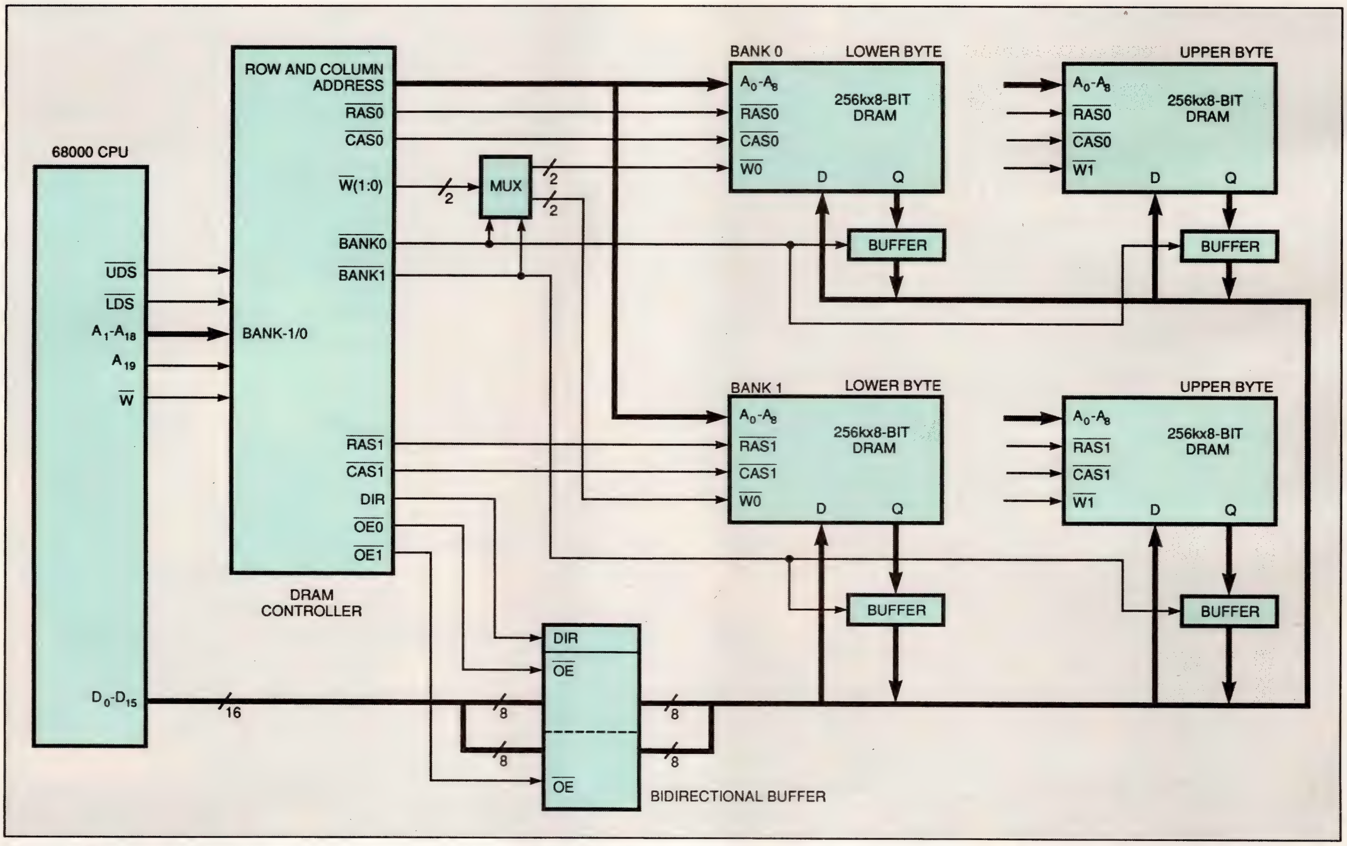
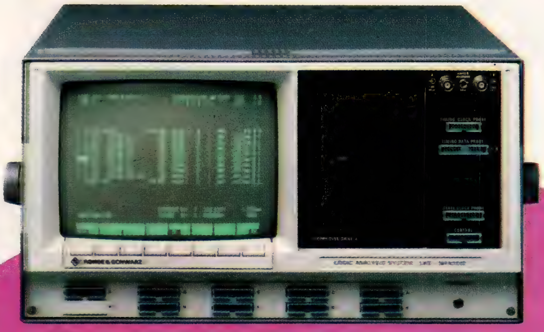



***Fig 7—To use static-column-access mode,** you must put each bank in the memory system into a bank-oriented-CAS configuration. However, you must muliplex the $\overline{\text{WRITE}}$ lines between the memory banks by using bank-select lines ($\overline{\text{BANK0}}$ and $\overline{\text{BANK1}}$).*

# Modular Logic Analysis System



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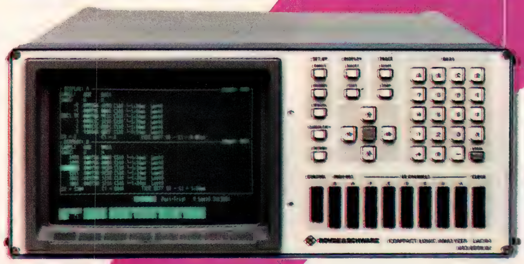

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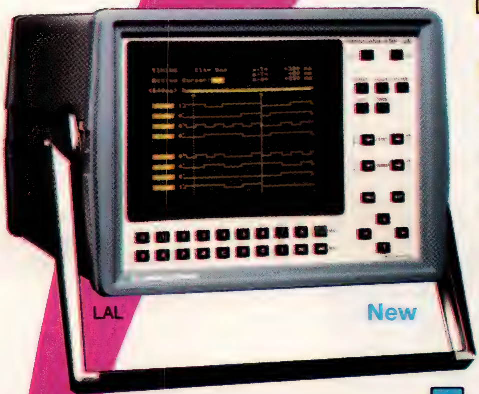

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# Following simple rules lets embedded systems work with μP emulators

*You can get a lot of mileage from a μP emulator, but finding that your system crashes when you connect the emulator is frustrating. Observing some simple rules at the outset of a new design can forestall crashes, speed debugging, and let you use emulators in test and service.*

Arnold S Berger, *Hewlett-Packard Co*

Microprocessor emulators are invaluable tools in the design, production, and maintenance of systems that contain embedded processors. Emulators are potentially useful not only in software design—where an emulator can run "out of circuit" by using its internal emulation memory—but also in software/hardware integration and even in test and maintenance. However, many engineers find that, despite their promise of improved productivity, emulators work well only in highly specialized tasks.

One reason for this state of affairs is that designers of μP-based systems often create products without giving any special consideration to the needs of emulation. The designers of μP emulators try to make their products affect the operation of the system under test as little as possible, both mechanically and electrically. But there are many things that digital design engineers can, and in some cases must, do to make their designs "friendlier" to emulators.

Almost every advertisement for emulators and development systems shows a single printed-circuit card on an immaculately clean bench top. The emulator or emulator pod sits conveniently next to the pc card with its 8- to 10-in.-long cable neatly plugged into a socket on the pc card or the target system.

In the real world of embedded-systems design, the μPs are truly "embedded." Actually, "buried" is a more accurate description. Typically, the processor is located in a random location on the pc card and in a random orientation. The word "random" is actually misleading because laying out a dense pc card is hardly a random process. Nevertheless, when placing and orienting the embedded processor, the person responsible for the layout probably gives little or no thought to the mechanical design of the in-circuit emulator that the electrical designer will use for debugging. A simple example illustrates this point.

**Fig 1** is a schematic representation of a fairly typical electronic system. The pc cards are contained in an equipment rack; they communicate with each other over a passive mother board or backplane. Designs that permit the use of extender cards greatly improve access to the processors. However, even if the circuits operate reliably on extender cards, the orientation of the processor with respect to the target-system interface cable can still prevent you from plugging in the emulator.

For example, the 68000 μP is usually packaged in a DIP. Many emulator manufacturers use a flat insulation-displacement cable to connect the emulator to the

*Too often, designers of μP-based systems create products without giving special consideration to the needs of emulation.*

target-system plug. The width of this cable is usually the same as the length of the DIP plug—about 3 in. Unless you can align the emulator almost perfectly with the plug and the target system, you will lose a significant portion of the useful length of the cable because it will have to make several 90-degree bends. In some cases, the cable won't be long enough to reach the plug, and you'll be out of luck.

In the 64700A series of emulators, Hewlett-Packard chose to make the cable very narrow—less than 1-in. wide on most emulators in the product family. The cable enters the 64-pin DIP plug at the end between pins 32 and 33. The designers chose this location because market research showed that in many applications ICs are positioned on a pc board with their longer side along the axis between the front and back of the card. However, if pin 1 faces back toward the emulator rather than toward the mother board, the cable will have to make a 180-degree turn to plug in properly. Even with the extended probe length of the 64700A family, going "around the bend" can use up a lot of cable length.

Many circuits will not work properly if the circuit cards are extended from the mother board. Sadly, this situation is becoming more commonplace as processor clock rates extend past 20 MHz and burst modes lead to one data cycle per clock cycle. In these cases, if you locate the processor near the outside edge of the pc card, you may still be able to plug in the emulation probe.

Sometimes there are mechanical quirks that can aid in emulation. The 80186/80188 processor family is available in both leadless-chip-carrier (LCC) and pin-grid-array (PGA) packages. You can buy sockets of both types that have exactly the same pin configuration and that use the same amount of pc-board space. The processor itself is less expensive in the LCC version, but LCC sockets are both more expensive and—in applications like emulation that involve large numbers of insertion/withdrawal cycles—less reliable than are PGA sockets. Using a PGA socket allows a more reliable and less expensive emulation connection. Once the emulation phase is complete, you no longer have to frequently mate and unmate ICs and plugs from the socket. If you selected the correct sockets, you can then produce the board with an LCC socket and an IC—a combination whose cost is less than that of a PGA socket and a μP (**Fig 2**).

As mentioned before, the coming generations of processors have clock speeds greater than 20 MHz,

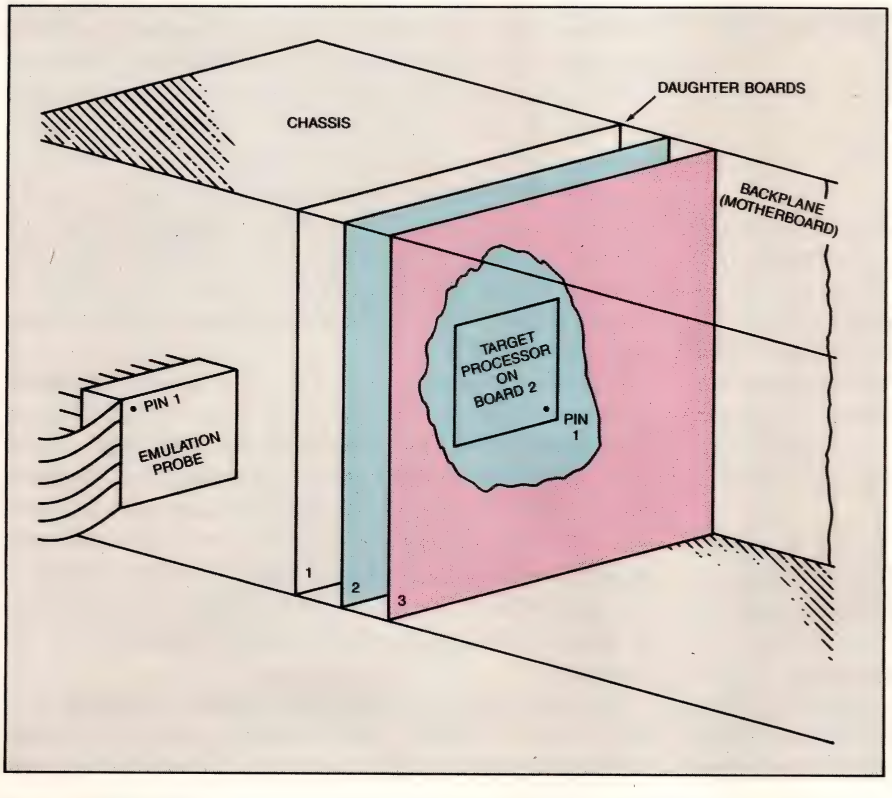



***Fig 1—An emulation nightmare:** The target processor is deep on daughter board 2. Another circuit board, ¾-in. above board 2, forces you to access the μP from the open board end. Unbuffered, high-speed signals traveling between boards via the backplane rule out the use of a card extender. To make matters worse, the target processor socket orientation makes connecting the emulator cable next to impossible.*

with 30 MHz becoming commonplace. Their data rates are approaching 240M bytes/sec. The emulation of such processors demands the use of active-probe technology, and the use of active probes places new demands on the emulator designer and the embedded-processor-system designer.

For example, when using an active-probe plug that occupies an area of roughly 6 to 9 in.$^2$, it's critical that you allow enough room to properly seat the probe in your board. Components near the processor may prevent the processor from plugging into the socket. With slower processors, you could always plug in extender sockets to permit the plug to clear the board. However, at 30 MHz you must consider the inductance and distributed capacitance of the connections between the μP and the rest of the system. (Yes, these are analog effects.) Stacked sockets simply don't provide the correct characteristic impedance for signal transmission or a low enough impedance for good ground return paths.

You may have to probe other parts of the circuit in addition to the processor. If the circuit packaging is quite dense and you have failed to provide adequate test points, you may be unable to make certain types of critical measurements.

### Surface mounting poses more problems

Boards built with surface-mounted components often present probing problems. For example, consider a board containing a digital-signal-processor (DSP) chip that operates as a slave and a general-purpose processor that acts as a master. The two chips operate in a tightly coupled mode, sharing a common bus and memory. Data moves in blocks from one chip to the other via coordinated DMA transactions.

Suppose that data at the end of the blocks is becoming corrupted; you suspect a timing glitch or a metastable state in your sequencing gate array. The HP 64700A family lets you connect an optional, 16-channel state/timing analyzer to other circuit nodes in the target system by using conventional logic-analyzer probes. This external analyzer is actually an extension of the HP 64700A's internal bus analyzer. You can completely couple the external analyzer to the internal μP instruction sequence that leads to and brackets the event under scrutiny. Thus, when the DMA handshake sequence begins, the internal bus analyzer arms the external timing analyzer, and the external analyzer records the external events. However, you can't make this straightforward and powerful measurement if you haven't provided the test points for the critical nodes.

These mechanical considerations suggest electrical problems that you must keep in mind when you design a pc board. For example, although designers of emulators try to bring a high degree of transparency to their products, they still have to depend on the target-system designer's adhering to the timing rules for the target processor. Most ICs will work beyond their published timing limits, at least at room temperature. However, the emulator designer needs every available nanosecond to perform design tricks. Therefore, design to your μP's published specs. If you don't, you're courting disaster on two fronts: Under some environmental conditions, the μP may not operate reliably, and your emulator is even less likely to operate reliably.

Sometimes, the emulator steals several nanoseconds

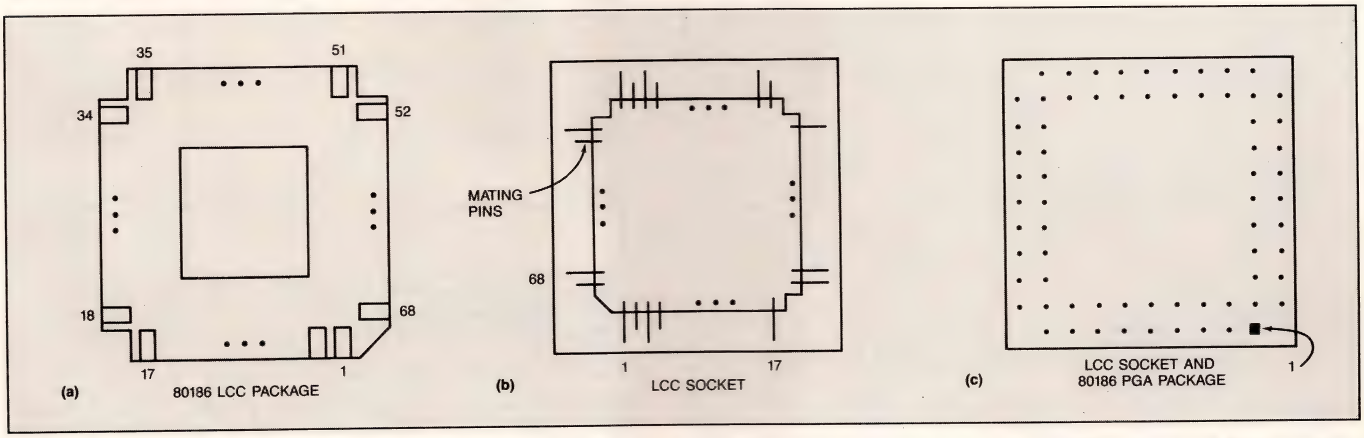



*Fig 2—The 80186 LCC package (a) and the 80186 PGA package are quite different. However, you can buy LCC sockets and PGA sockets with identical pin configurations. The diagram in b is a view of the component-insertion side of the LCC socket; c is a view of the side of either socket that mates with the pc board. You can easily use the PGA socket during emulation and convert to the LCC socket in production.*

*Typically, the processor is located in a random location on the pc card and in a random orientation.*

from, for example, a memory-access cycle. Usually, the emulator needs this time to send a signal up and down the cable and to pass signals through the buffer, the cable drivers, and the receivers. If you understand the performance of your emulator in detail, you can sometimes circumvent problems that result from the emulator's internal delays by simply replacing the standard memory chips in the target-system prototype with faster parts. Such a substitution can make the difference between a reliable design/emulation system and one that "goes into the weeds" at the most unexpected times.

Another famous "gotcha" is the wire-wrapped prototype. These units are often 3-D designs with nonexistent power and ground management. Wire-wrapped boards may actually work with a processor chip in place but "die" when you plug in the emulator. Again, the explanation is the failure to consider the emulator and the target system together as a larger system.

To preserve the edge speeds on the signals it supplies to the target system, the emulator uses heavy-duty, line-driving buffers to drive its cable. If the power and ground systems have excessive inductance, there is no low-impedance path for current returning from the target system to the emulator. As a result, voltage pulses appear in various signal lines at odd times—a phenomenon often called "ground bounce." Some of these pulses exceed the switching threshold of parts on the target system or the emulator itself. **Fig 3** shows a schematic representation of the emulation-probe/target-system interface; **Fig 4** shows an actual ground-bounce waveform. **Ref 1** discusses this phenomenon in greater detail.

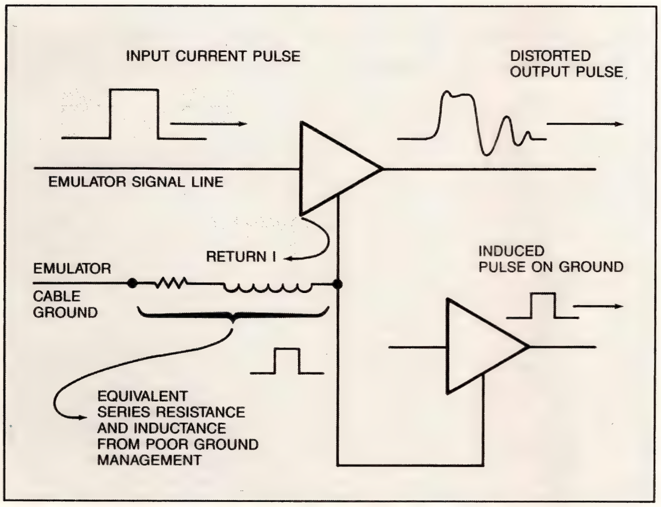



***Fig 3—Poor control of the ground return currents** leads to distorted and spurious signals at the emulation-probe/target-system interface. The high current capability of the emulation probe's drive circuits exacerbates the problem.*

**Simple damper improves reliability**

Emulator designers would love to demand that every target system use a 4-layer pc board with power and ground planes, but target-system designers just won't comply. Economic considerations often dictate that in the finished product you use a 2-layer, or even a single-sided, board design with marginal power and ground traces. In digital-system prototyping, wire wrapping and its variations are a way of life. **Fig 5** shows a solution to the problems caused by such construction—a simple "damper" socket for a Z80-based system. You place the damping resistors in the critical signal lines; they serve to damp out the fast edges of the signals traversing the cable. Typical resistor values are between 10 and 100Ω; higher resistances provide more damping. A good starting value is 22Ω. This simple circuit modification produces dramatic improvements in target-system reliability.

Some of the newer processor chips provide built-in

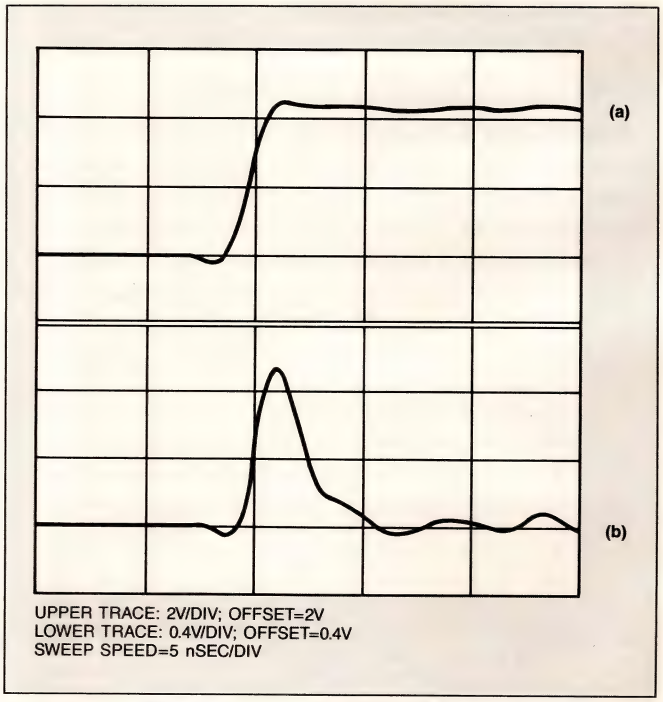



***Fig 4—Referenced to emulator-probe ground,** "ground bounce" caused by poor ground management can be large enough to cross the threshold of a TTL device. The fast 2V edge, **a,** causes a pulse nearly 1V in amplitude from a 0.4V baseline, **b,** on the target-system ground.*

emulation help. For example, Advanced Micro Devices' 29000 RISC processor incorporates features that ease emulation. If emulator designers could count on the use of such features by all target systems, they would be able to achieve many emulator-performance improvements. However, target-system designers usually ignore such processor features or view them as imposing unrealistic restrictions. Today, you often hear about "design for testability." "Design for emulation" is the same idea.

Part of the process of selling an emulator is the ritual Plug-in Demonstration. The poor salesperson goes to a customer site and hears, "I'll buy your emulator if it works in my target system." The salesperson then plugs the emulator in and hopes for the best. Such an exercise does relatively little to demonstrate the emulator; what it demonstrates is a limited viewpoint on the part of the prospective purchaser. Obviously, the emulator should work in a target system, but there are many other tools that contribute to the overall usefulness of a μP development system. The emulator is just a part of the design chain. It's false economy to make a development-system purchase decision solely on the basis of the emulator's performance on a board you have already designed.

Here is an alternate scenario. As part of the overall strategy for designing a new product, you choose a development system and support software. Your choices include an integrated set of compilers, debuggers, assembler/linkers, user interfaces, emulators, and support and verification tools. The hardware designers or the hardware/software-integration-team members study the features of the emulator and note possible performance limitations. They propose work arounds as part of an overall purchase decision. For example, suppose that the target system contains a watchdog-timer circuit that generates an interrupt at regular intervals. Emulators often fail in such situations because certain modes of operation prevent them from handling interrupts correctly. Designers who understand this mode conflict can make a straightforward addition to the design to permit disabling the watchdog timer during emulation.

Again, designing for emulation in the early stages of a project keeps you from finding yourself in a corner in the later stages.

When making your software compatible with emulators, remember this prime commandment: Modularize, modularize, modularize! Modern programming languages are wonderful for writing compact, testable, and maintainable code. The compact modules of code they produce are an excellent match for the feature sets provided by the emulation memory in most modern emulators. These emulators let you map or overlay blocks of emulaton memory onto actual areas of the target system's memory space. An obvious use of this

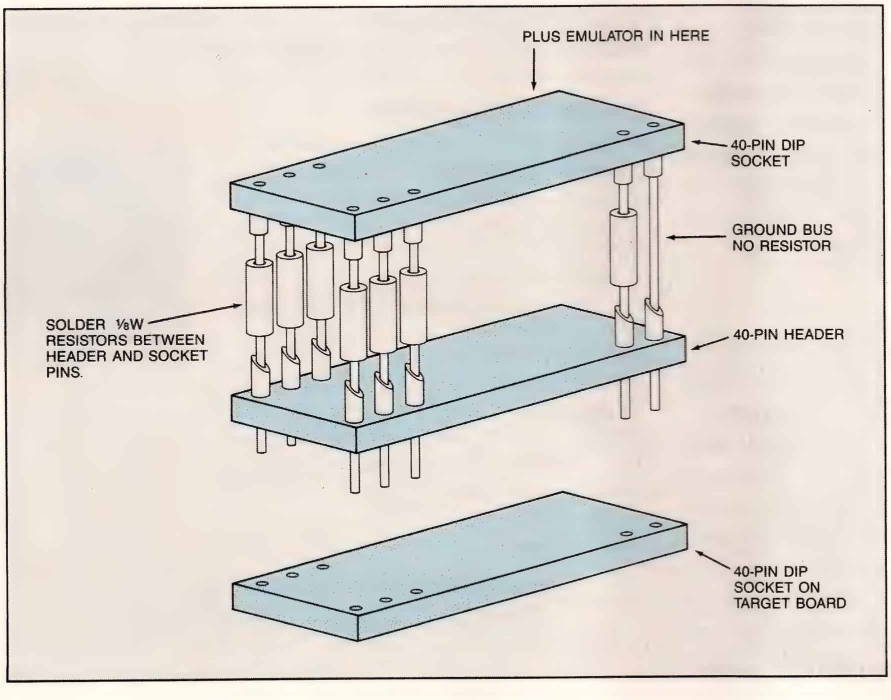



***Fig 5—A homemade damper circuit*** *is an effective means of slowing down fast edges from emulator probe cables. Typically, you will need to damp the address, data, strobe, and clock lines.*

*Unless you can align the emulator almost perfectly with the plug and the target system, you will lose a significant portion of the useful length of the cable.*

feature is in eliminating the need for ROM in the system under development. But unless the code modules lend themselves to the overlay process, you won't realize much of the emulation memory's value.

Consider the situation in which an emulator manufacturer supplies emulation memory in 128k-byte increments and the anticipated size of the final code is about 512k bytes—a value typical of laser printers. One solution to this seeming lack of emulation memory is the purchase of enough emulation memory to cover the entire application space. The idea is wonderful if the cost of high-speed static memory is not a problem. In fact, emulator vendors would love to sell billions and billions of bits of static RAM. However, in most cases large amounts of emulation memory are an unnecessary luxury. By keeping code modules small and self-contained, you can easily develop the entire product in—pardon the pun—byte-size chunks. (Obviously, the chunks are somewhat larger than one byte.)

Another example of the advantage of modular code is the HP 64700A family of emulation products, which provides coverage analysis of emulation memory. This verification tool is a simple but useful one for software designers. The coverage memory records every read or write access to a block of emulation memory. Thus, it can tell you if you're exercising all of the code. If the code modules can stand on their own, with well-defined boundaries between the modules, you can test a block of code with full confidence that you have examined all possible methods of accessing the block. In fact, emulator manufacturers use this feature for the final software qualification of their emulation products. Even if a particular product contains several million bytes of code, the vendor can "walk" the tests through the emulator's entire memory space by keeping the modules and their associated libraries within the bounds of the available emulation memory.

### You need emulation, so design for it

Unlike most embedded-system designers, analog designers have long recognized the need to consider the design constraints imposed by test and measurement equipment. These engineers routinely pair signal and ground test points to ensure good fidelity in rise- and fall-time measurements. Taken in that spirit, these suggestions should aid embedded-system designers. For example, if you can locate the processor chip in a mechanically convenient location, do so *before* you do your pc-board layout. Otherwise, you can end up locked into a situation you can't live with. If you don't consider the emulator's requirements early in the design of your product, you'll need to make the length, size, and flexibility of an emulator's cable part of your emulator purchase criteria.

Looking into the future, the trend toward increased modularity in software design bodes well for the future of emulation. On the hardware side, though, the picture is not as rosy. Faster, higher-performance processors impose increasingly stringent requirements on both emulator hardware and target-system pc-board layouts. By listening carefully to designers of embedded systems and engaging in a continuing dialogue with designers of IC components, emulator designers are doing their part to create instruments that can handle these tougher requirements. Now it's the embedded-system designers' turn. Unless they listen to emulator designers and heed the concepts of design for emulation, there's a good chance that they will deny themselves the benefits of μP emulation in the development, manufacture, and support of future generations of μP-based systems. **EDN**

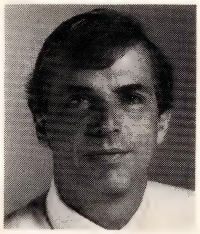
## Reference


1. Peurifoy, Steven W and Arnold S Berger, "Cabling technology vital to high-end emulator performance," *Personal Engineering and Instrumentation News*, November 1988, pg 47.


## Acknowledgment


The author is grateful to Steve Peurifoy for the use of the results from his emulation-cable-technology study.


## Author's biography



*Arnie Berger is a project manager responsible for Hewlett-Packard's 64700 series of emulation products at the company's Logic Systems Div in Colorado Springs, CO. He has been at HP for 10 years; previously, he worked at Ford Motor Co and Argonne National Laboratory. Both his BS and PhD degrees are in materials science from Cornell University. Arnie is a member of the American Physics Society and has published or presented over 30 papers. His leisure activities include bicycling, running, and woodworking.*

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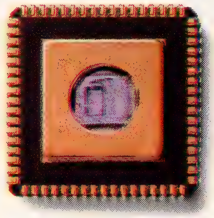

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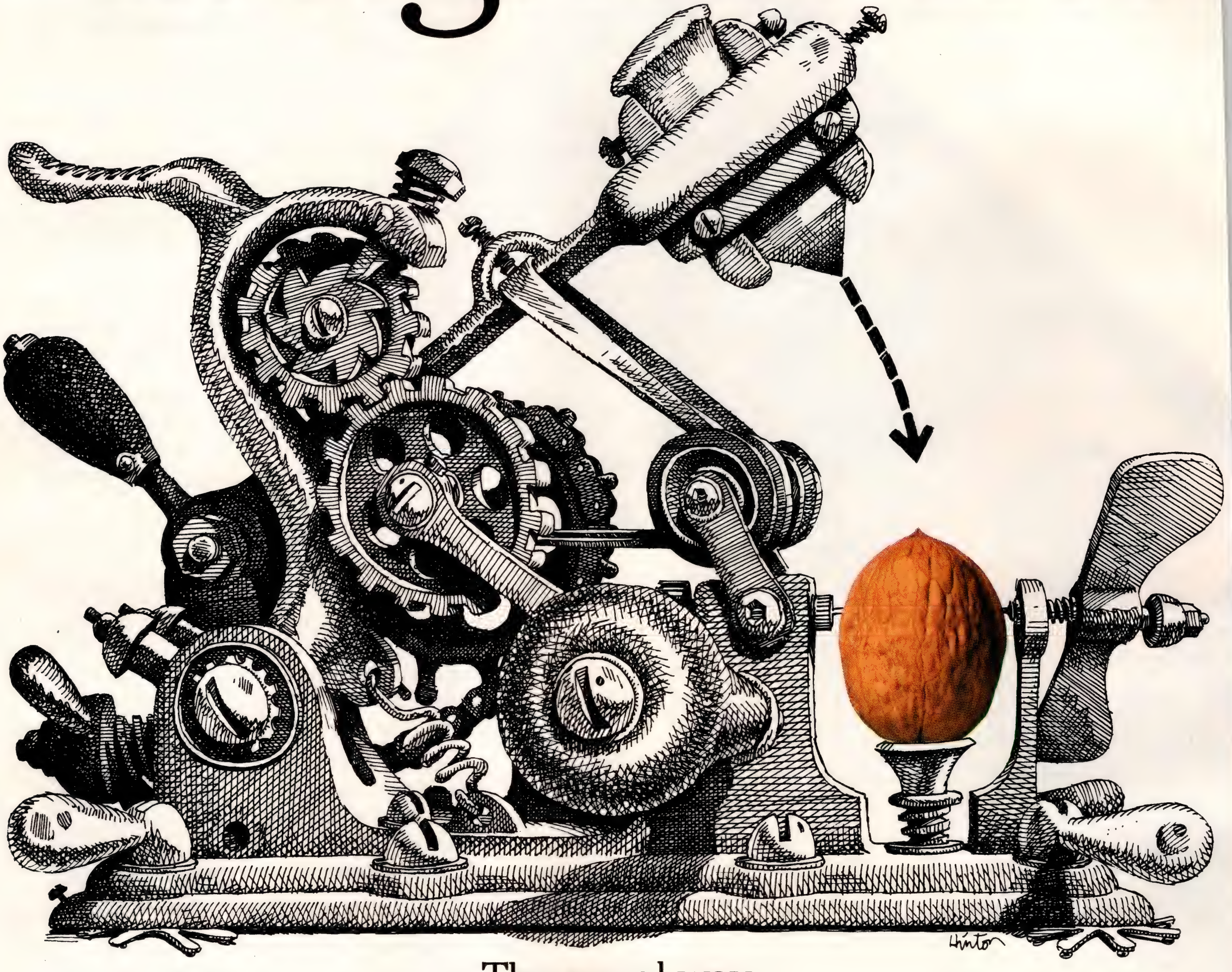

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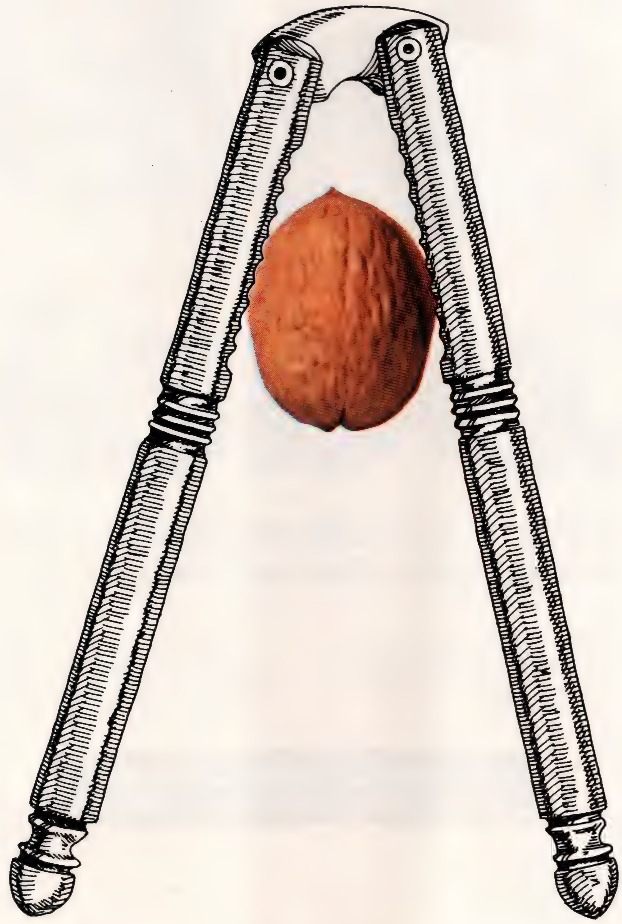

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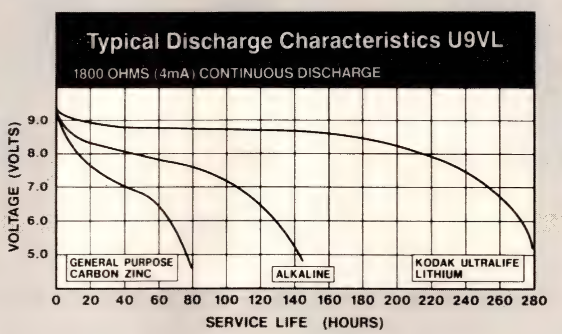


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# Stimulus-response tests are easy with an 8-bit µP

*Despite its association with large and costly test systems, stimulus-response testing is actually simple and straightforward. You can build a low-cost stimulus-response tester around an 8-bit µP and easily adapt it to a remarkably wide variety of tasks.*

Paul D Gracie, *Microdoctors Inc*

Stimulus-response (SR) testing is a well-known technique frequently used in large, high-speed automatic-test systems. In an SR test's simplest form, the controlling CPU reads a test-stimulus value from its memory and sends it to the device under test. After waiting for the system to respond, the processor reads the response and stores the value in a new group (block) of memory locations. When the test is completed, the processor compares the results with a known-good response pattern to detect errors.

You can apply this general method to many other types of tests, such as a stimulus-comparison (SC) test. The minimum equipment you need for SR testing is neither unusually complex nor particularly expensive; you can program a small microcomputer to do simple SR tests. Moreover, you can easily adapt the concept to almost any microcomputer system.

The hardware used for the sample tests is a single-board, 8085-based microcomputer system called the TC-100 (**Fig 1**). It has 8k bytes of PROM, 2k bytes of RAM, an RS-232C serial port, and an 8255-based parallel port. SR testing uses the three 8-bit parallel ports as follows:

Port A: Response Input
Port B: Stimulus Output
Port C: Control Output.

The Port C output sets the static control values and contains one bit that acts as a data strobe for the stimulus output.

The basic operating system is a control monitor called Swan, which, along with the usual memory and I/O control routines, has a number of modules written

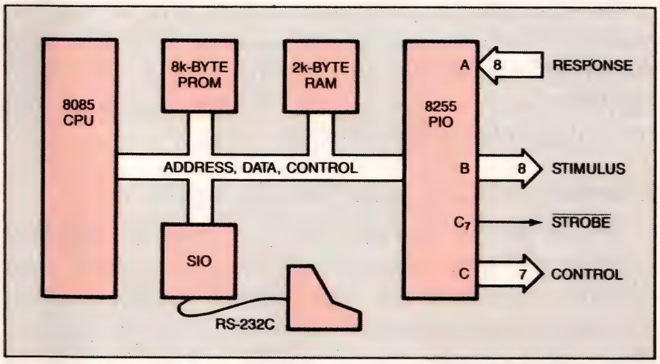



***Fig 1—The test-computer block diagram** illustrates the parallel I/O port used for SR tests.*

*Routines optimized for speed can operate at rates in excess of 100,000 operations per second.*

for electronic testing. The monitor also has many features that simplify program setup and operation—for example, memory-reference labels, automatic block sizing, automatic pattern generation, and a single-step mode.

The monitor contains three commands for SR testing:

SR <BLOCK><ADDRESS>[<DELAY>] <cr>,
SC <BLOCK><ADDRESS>[<DELAY>] <cr>,
and SL <BLOCK>[<DELAY>] <cr>,

where "<cr>" denotes a carriage return. The SR command outputs data from <BLOCK>, waits a <DELAY> (whose optional nature is denoted by brackets), and writes the result to a block beginning at <ADDRESS>. The SC command outputs data from <BLOCK>, waits an optional <DELAY>, and then compares the result with the data stored in the block beginning at <ADDRESS>. If the result of the comparison is true, the program continues to the next address. If the result is false, the program dumps the output, comparison, and input values to the terminal and then continues. The SL (stimulus-loop) command outputs the contents of <BLOCK> into a loop with an optional <DELAY>. The SL command thus generates digital waveforms.

## The command syntax is straightforward

Using the facilities of the monitor, most commands take the form SR R T <cr>. That is, the commands output a 256-byte stimulus word contained in the block of memory that begins at R (2000 hex) and write the result to block T (beginning at 2400 hex). Once you set the stimulus pattern, operation of the program is very simple.

The routines do I/O transfers at a rate of approximately 10,000 operations per second. Routines optimized for speed can operate at rates in excess of 100,000 operations per second. For greater speed, you can build a high-speed interface.

## Interfaces to units under test are simple

To use the SR function, you can build an interface between the test computer and the device under test, develop a test pattern, and enter the pattern along with the proper command. All of the following applications use a simple, 256-byte pattern that increments from 0 to FF hex. In addition to counting, this pattern produces square waves.

You can develop more complex patterns and use the monitor to write the patterns to the µP's memory, or you can burn them into a PROM for a permanent record. For SC tests that require comparison patterns, you can write the pattern to RAM using the monitor, or you can use the SR command and a known-good device to generate the pattern.

## The tester checks cable continuity

The interface shown in **Fig 2** tests and maps cables that have as many as 16 conductors. In operation, the

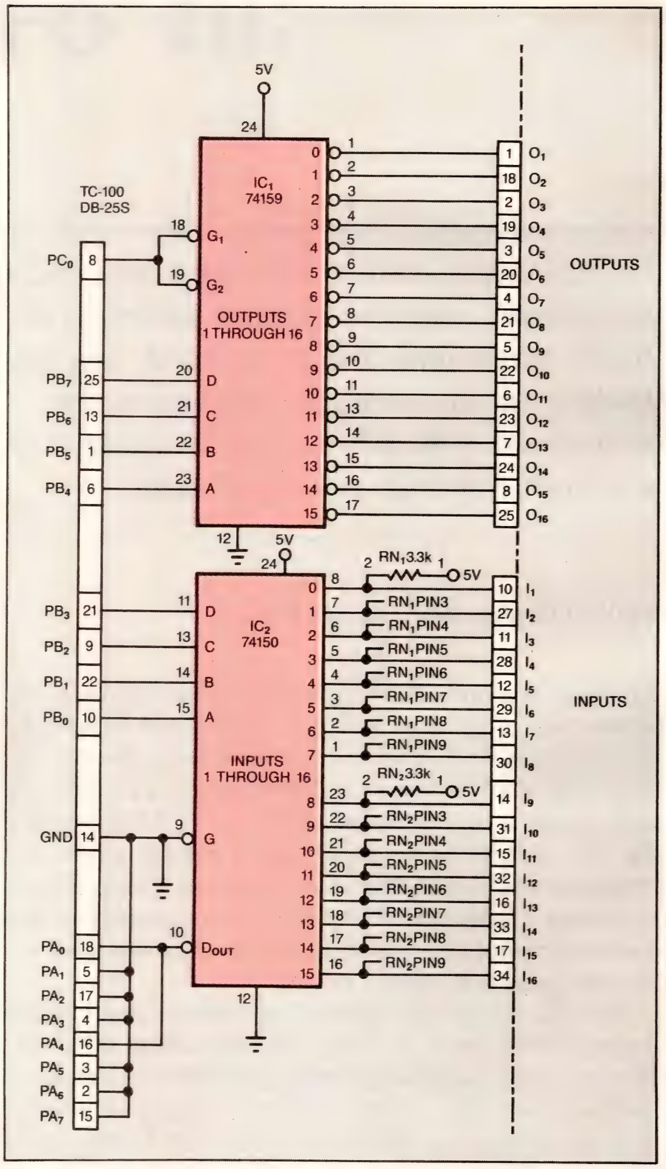



*Fig 2—In the cable-test interface, $IC_1$ drives the cable with one logic-0 level at a time while $IC_2$ scans the cable for connections.*

74159, $IC_1$, drives one of 16 outputs low; the 74150, $IC_2$, scans all 16 inputs and saves the result in memory. When the 16-step scan is completed, $IC_1$ drives the next output low, causing $IC_2$ to repeat the scan. At the end of all 256 steps, the memory contains a map of all of the cable's end-to-end connections. Note that this test won't detect connections between pins of the same connector unless the connections exist within the cable. The response provides a distinctive pattern of 00 for no connection and 11 for a connection. If you use the monitor's hex-memory-dump command, the screen shows a $16 \times 16$-point map of all end-to-end cable connections.

Using the SC command, you can quickly test a large group of cables. After you set up the system, attach the interface to a known-good cable. Run the SR command to put a known-good map into memory. Then attach the interface to a cable that you want to test and run an SC command. If the cable is good, the system returns the prompt. If the cable is defective, the system prints an error message in the form NM XX YY: N is the output pin number, M is the input number, and XX YY indicates the type of defect. The pattern 11 00, for example, indicates a missing connection, and 00 11 denotes a shorted connection.

You can read most types of PROMs by building an interface consisting of only a socket for the PROM. The interface shown in **Fig 3** works with 27xxx PROMs. Again, the stimulus pattern increments from 00 to FFh. This pattern provides the lower address bits, $A_0$ through $A_7$. The port C outputs supply the upper address bits, $A_8$ through $A_x$. The $\mu$P reads data from the PROM as a response pattern to the address stimulus and stores the data in the response RAM. You can then view the data by using the monitor's display-memory command. You can read any 256-byte page of the PROM by setting the proper page number onto the Port C output.

**Measure relays' maximum operating speed**

You can use this system to test electromechanical relays for both function and speed. The interface required varies with the type of relay tested, but in most cases, it is as simple as the one shown in **Fig 4.** The interface consists of a transistor driver for the relay coil, a socket for the relay under test, an interface to the computer, and a power supply. The stimulus pattern, which is the same incrementing pattern discussed previously, is used as a square-wave source to drive the relay coil. For a 256-byte pattern, the system drives the relay through 128 on/off cycles and records the contact condition for each half cycle. The response memory pattern is a 22 11 22 11 . . . series for a good relay; the 2 signifies an open contact, and the 1 denotes a closed contact. A 3 in the pattern means that a completely open (floating) contact is present, and a 12 or 21 shows that a shorted contact exists.

Because electromechanical relays don't cycle at a

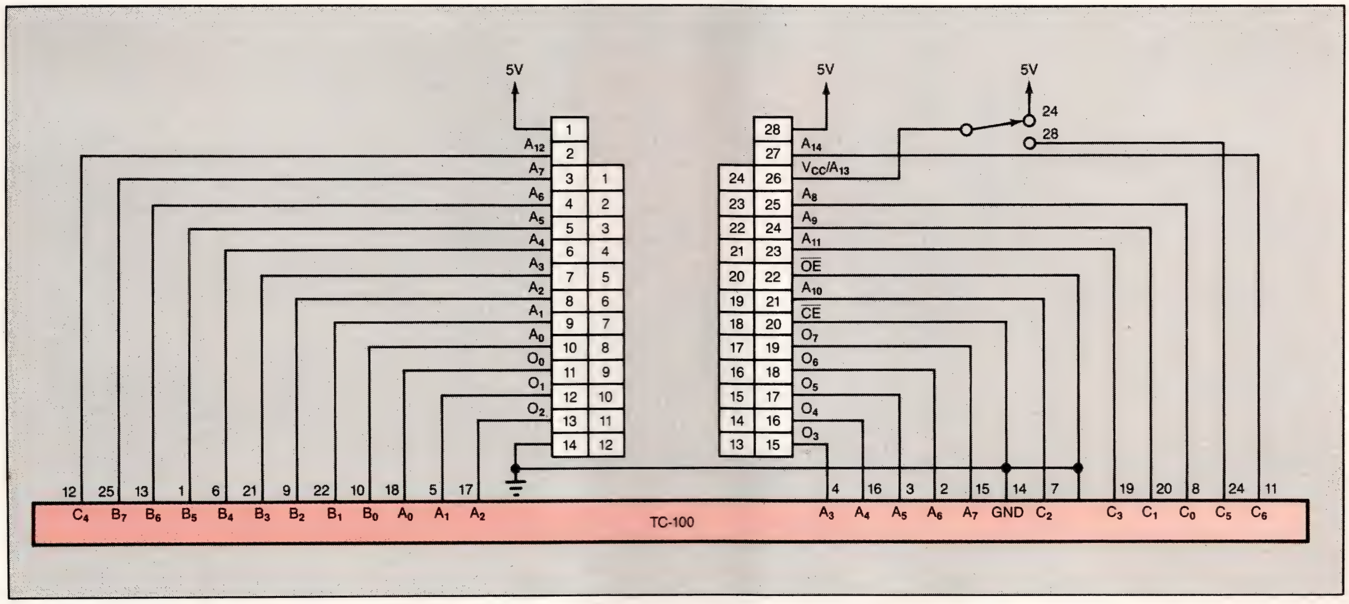



*Fig 3—**To read 27xxx PROMs,** you can use an interface that consists of just a socket connected to the ports.*

*To use the SR function, build an interface between the test computer and the device under test, develop a pattern, and enter the pattern along with the proper command.*

rate of 5,000 operations per second, you must specify a delay when entering the SR command. The following procedure lets you determine the proper value of the delay setting for a particular type of relay. The test computer generates a base delay of 196 μsec and an incremental delay of 16 μsec per step. For preliminary testing, specify the delay with the command SR R T FFF. With this delay, the relay operates at 65.7 msec per cycle—a speed low enough to guarantee that most relays will operate reliably. This SR test produces a known-good response pattern and loads it into the response RAM. You can then use this pattern for a speed test. Your attempt to find the maximum reliable operating speed of the relay might produce results like these:

| | |
|---|---|
| #SC R T 900 ; | RELAY ALWAYS PASSES AT 37.04 mSEC/CYCLE |
| #SC R T 800 ; | CONTACT SET A FAILS AT 32.94 mSEC/CYCLE |
| #SC R T 700 ; | BOTH CONTACTS FAIL AT 28.85 mSEC/CYCLE |

When you run the test at various speeds, the system returns the prompt if the relay passes, and it prints the errors if the relay fails. You can also run this test using a variable power supply to determine the pickup and dropout voltages of a relay under various drive conditions.

With a minimum delay of 196 μsec, the test computer is not fast enough to test high-speed logic at full speed. To overcome this limitation, you can build a simple, high-speed interface, which is shown in **Fig 5.** This interface consists of a one-shot ripple counter that is triggered by the stimulus data strobe. The interface shortens the SR test time by compressing the SR cycle. Operation of the interface is as follows:

**Setup:** At power on, a short low pulse (*POC) clears the shift register, $IC_6$, and sets $IC_8$, pin 9 high, enabling the clock. Because all outputs of the shift register are low, $IC_5$'s output is high, and successive clock pulses shift the high state to the outputs $Q_A$ through $Q_G$. When outputs $Q_A$ through $Q_G$ are high, $IC_5$, pin 8 becomes low. This low output, inverted by $IC_3$, triggers a short pulse on $IC_8$, pin 5, which disables the clock by setting $IC_8$, pin 9 low. The circuit is now ready to operate: $Q_A$ through $Q_G$ are high; the data, $IC_6$, pin 1, is low; and the clock is off.

**Operation**: After setting the stimulus data on port B, the computer generates a low strobe on port C—bit 8. The rising edge of the strobe sets $IC_8$, pin 9 high

*Text continued on pg 188*

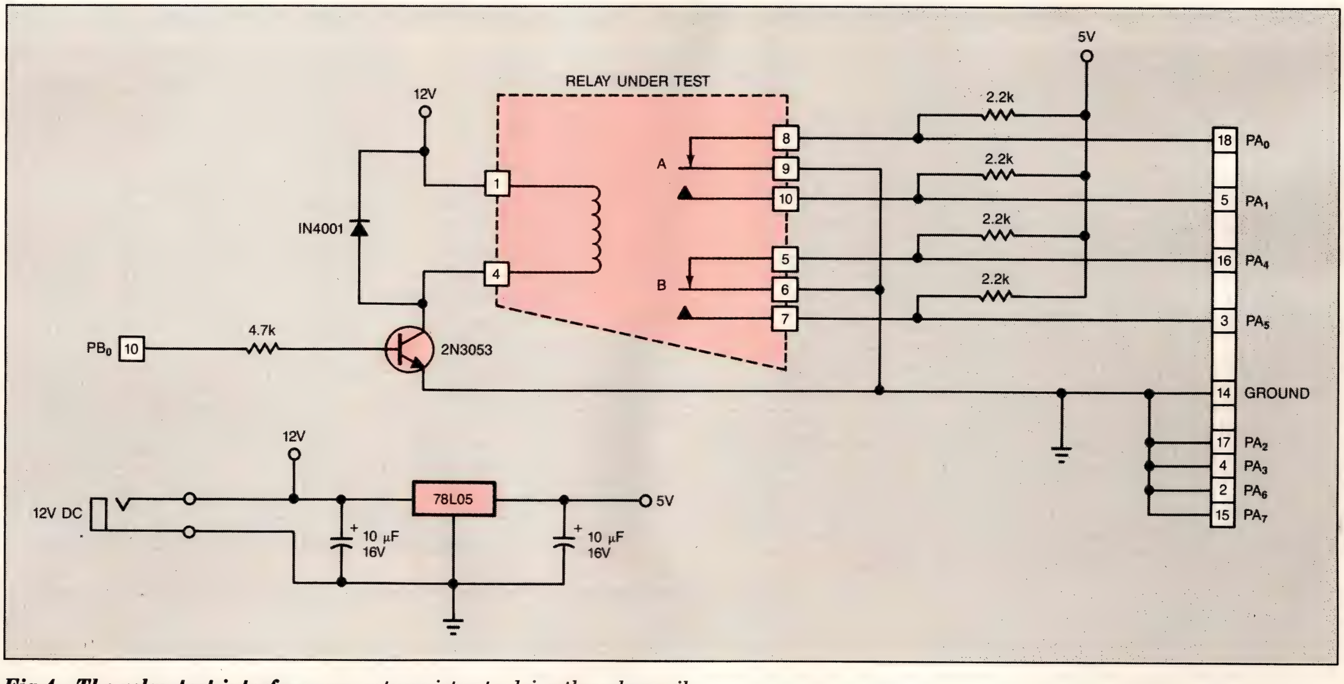



***Fig 4—The relay-test interface** uses a transistor to drive the relay coil.*

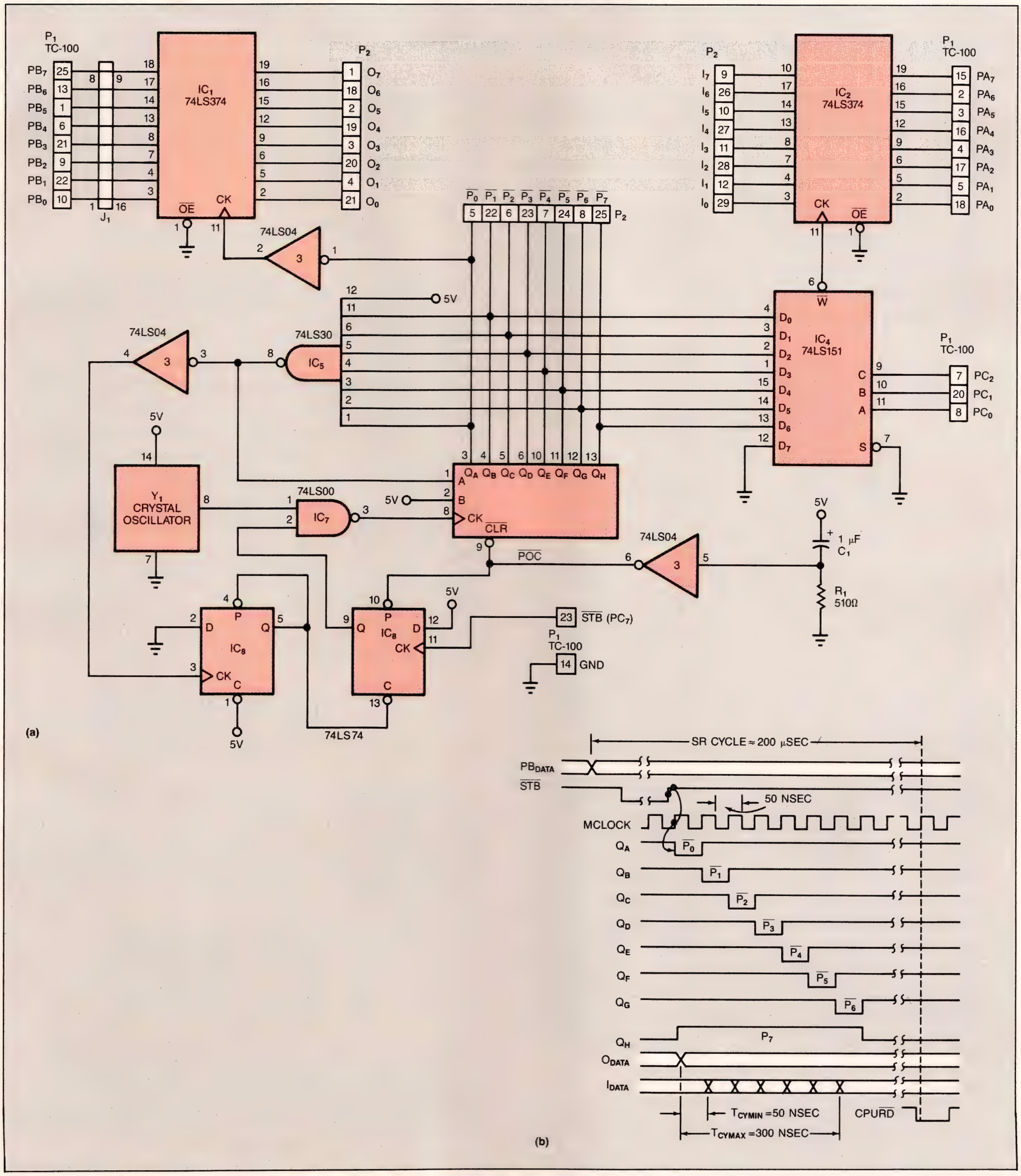



*Fig 5—The high-speed interface* ***(a)*** *is a one-shot ripple counter that uses a shift register to move a pulse* ***(b)*** *to the stimulus and response registers at high speed.*

## Stimulus-response software can be straightforward

It's relatively simple to create software suited to stimulus-response (SR) testing for most microcomputers. In general, the software must maintain two pointers—one for the stimulus address and one for the response address. These pointers direct data to and from memory for the test. After each SR cycle, the processor increments the pointers and compares the stimulus pointer to an end value. The program then loops for the next cycle or exits for termination. The program follows the form

```
SR   : INIT                ;INITIALIZE POINTERS
       MOV   A, (SMEM)     ;GET FIRST STIMULUS
LOOP:  OUT   STIMPORT      ;OUTPUT STIMULUS
             (DELAY)       ;DELAY ADDED HERE
       IN    RESPPORT      ;INPUT RESPONSE
       MOV   (RMEM), A     ;SAVE RESPONSE
       INC   (SPNTR)       ;INCREMENT STIM ADDRESS
       INC   (RPNTR)       ;INCREMENT RESP ADDRESS
       TEST  END           ;TEST END ADDRESS
       RET   DONE          ;RETURN IF DONE
       MOV   A, (SMEM)     ;ELSE GET NEXT STIM
       JMP   LOOP          ;AND LOOP FOR NEXT.
```

The program must first initialize the pointer registers with the start addresses of the stimulus and response blocks. To simplify the setup procedure, the program can use fixed address values and read the stimulus data set from a PROM. Using this method, you can make a "pushbutton" SR test. The first stimulus data value moves from memory to the accumulator and then out the stimulus port. At this point in the program, you can add a delay to provide time for slow devices under test to respond to the stimulus. After the delay, the program reads the data on the response port, saves it in the response memory, increments both pointers, and compares the stimulus pointer with the end value, which equals the last stimulus-block address plus one. If the result of the comparison is false, the program loads the next stimulus value into the accumulator and loops until it receives the next stimulus output. If the result is true, the SR operation is complete and the program returns to the calling routine.

### You can calculate response time

The microprocessor clock speed and the number of clock cycles required to complete one turn of the program loop determine the timing of the SR operation. Two timing values are important: the stimulus-to-response delay and the response-to-next-stimulus dwell. The minimum time required to increment and test the pointers plus the loop-close time establish the dwell time. You can determine the dwell time from

$$\text{DWELL} = (\#\text{CC} \times \text{CP}) - \text{DELAY},$$

where DWELL is the dwell time, #CC is the number of clock cycles in the loop, CP is the clock period, and DELAY is the stimulus-to-response delay.

For 80-series processors, the stimulus-to-response delay equals one-half the sum of the output and the input cycle times; for other microprocessors, the delay can vary. For an 80-series processor, the minimum delay is 10 clock cycles; for an 8085 running at 3 MHz, the delay equals 3.333 μsec. To obtain the minimum delay, the input instruction must immediately follow the output instruction. For devices under test that require more time to respond to the stimulus, you must add a delay between the output and the input instructions. For very short delays, you can insert one or more dummy instructions between the output and input. For example,

```
LOOP:  OUT   STIMPORT   ;OUTPUT STIMULUS
             NOP        ;DUMMY FOR TIMING
             NOP        ;DUMMY FOR TIMING
       IN    RESPPORT   ;INPUT RESPONSE
                     MOV etc. . .
```

In this routine, two no-ops, which contain four cycles each, increase the delay time to 18 cycles (6.0 μsec at 3 MHz). You can implement longer delays by inserting a timeout loop between the output and input instructions. For example,

```
LOOP:  OUT   STIMPORT   ;OUTPUT STIMULUS
       MVI   A, DELVAL  ;GET DELAY VALUE
DLY:   DEC   A          ;DECREMENT DELAY
       JNZ   DLY        ;LOOP NOT DONE
       IN    RESPPORT   ;INPUT RESONSE
                     MOV etc. . .
```

The program moves a value, DELVAL, to the accumulator, decrements the accumulator to zero, and reads and saves the response. You can calculate the timing by

$$\text{DELAY} = (10 + 7 + ((4 + 10) \times \text{DELVAL}) - 3) \times \text{C P},$$

where

10 = the minimum number of cycles,
7 = the number of cycles in MVI,
4 = the number of cycles in DEC,
10 = the number of cycles in JNZ for jump, and
3 = the number of cycles JNZ is short for no jump.

The equation is shortened to

$$\text{DELAY} = (14 + (14 \times \text{DELVAL})) \times \text{CP}.$$

Assuming you use a DELVAL of 100 decimal and a 3-MHz clock, the total delay time is $14 + (14 \times 100) = 1414$ cycles $\times$ 333 nsec = 471.333 µsec. The maximum delay possible with this routine—$14 + (14 \times 256) = 3598$ cycles $\times$ 333 nsec = 1.199333 msec—occurs when DELVAL = 0 because the first DEC rolls the value over to FFh. You can obtain longer delays by inserting multiple loops or 16-bit loops in place of the simple loop shown.

You can simplify SR routines if you place some constraints on the form of the tests. For example, a program can easily calculate the incremental stimulus pattern used in some tests and thus avoid a sequence of memory-read operations. A routine that performs such a test can take the form

```
   SI: LXI  H, 2000  ;LOAD RESP BLK ADDR
       MVI  A, 0     ;LOAD FIRST STIM VALUE
 LOOP: OUT  STIMPORT ;OUTPUT STIMULUS
       IN   RESPPORT ;INPUT RESPONSE
       MOV  M, A     ;SAVE RESPONSE
       INC  L        ;INCREMENT ADDRESS AND STIM
       RZ            ;EXIT IF DONE
       MOV  A, L     ;ELSE GET NEXT STIM
       JMP  LOOP     ;AND LOOP.
```

This routine uses a fixed response-block start address of 2000 hex and requires 256 bytes of response RAM. Because the last two digits of the address start at 00 and increment in the same manner as the stimulus value, the same register that counts the address can also generate the stimulus. Because the program has to increment only one register, the start—at address XX00—and the 256-step cycle also simplify testing for the end of the routine. After the last test, the counter "rolls over" from XXFF to XX00, thereby setting the zero flag. Timing for this routine is

TOTAL LOOP = 51 CYCLES = 17 µSEC;
SR DELAY = 10 CYCLES = 3.333 µSEC
R/S DWELL = 41 CYCLES = 13.666 µSEC
SR TIME = 256 × 51 CYCLES = 4.352 mSEC,

where SR TIME is the total time for 256 SR cycles.

By following the general form of the examples given, you can write many other forms of SR test programs, which include

**Stimulus-comparison:** These routines compare the response to a known-good pattern and take action if the response doesn't equal the known-good pattern. When the test detects an error, the program can report the error and continue, or it can pause and leave the failing stimulus data in place to allow the operator to probe for the cause of the failure.

**Triggered-response:** These programs monitor a trigger port after the stimulus output and record the response only after they detect a specific trigger pattern. The programs can periodically increment a timer register to determine the time to trigger. They can store this value along with the response.

**Timed-response:** This type of routine applies a single stimulus and records a series of responses at fixed intervals over a fixed period. This test is useful for detecting differing response times of individual bits of the response word.

**Selected-stimulus:** On the basis of the last response, these routines select the next stimulus value from a list. They are similar to certain types of state machines. You can use these routines to simulate a state machine and to test the devices that the state machine controls.

**Single-step and manual-stimulus:** Programs that include these facilities are useful for static testing and for debugging failed devices. In particular, the single-step function is useful for tracing failures detected by a stimulus-comparison test.

*To overcome speed limitations, you can build a simple high-speed interface that includes a one-shot ripple counter triggered by the stimulus data strobe.*

and enables the clock. The first clock pulse shifts a low state on $Q_A$. This low state on $Q_A$ sets the data, $IC_6$, pin 1, high and loads the stimulus data into register $IC_1$, which feeds it to the device under test. The second clock pulse to the shift register moves the low state one place to the right—to $Q_B$. If the multiplexer, $IC_4$, has selected $Q_B$, the pulse then loads the response data into the response register, $IC_2$. The response register holds the data until the computer reads it. The low pulse continues down the outputs until it reaches $Q_H$. At that point, $IC_5$, pin 8 returns low, thereby shutting off the clock. The circuit is then ready for the next strobe pulse to start the process again.

The SR transfer delay for this circuit depends on the clock period of $Y_1$ and the propagation delays of $IC_3$ and $IC_4$. You can calculate the delay from

$$t_{td} = t_p + (t_{dr} - t_{ds}),$$

where $t_{td}$ = SR transfer delay, $t_p$ = clock period, $t_{dr}$ = response clock delay, and $t_{ds}$ = stimulus clock delay. The SR clock delays are the propagation delays of $IC_3$ and $IC_4$. When using a 20-MHz clock for $Y_1$, typical delays for the circuit shown are

$$t_{td} = 50 + (13 - 10) = 53 \text{ nsec.}$$

Note that if $t_{dr}$ and $t_{ds}$ are equal, the transfer delay is equal to the clock period, and if $t_{ds}$ is greater than $t_{dr}$, the delay is less than the clock period. For example, if you replace $IC_4$ with a wire and add a second inverter from $IC_3$, pin 2 to $IC_1$, pin 11, the transfer delay is

$$t_{td} = 50 + (0 - (10 + 10)) = 30 \text{ nsec.}$$

You can achieve very short SR transfer delays by selecting the proper stimulus clock delay.

You can use this interface to test multiple-rank devices, such as flip-flops and registers, because it generates seven pulses on $Q_A$ through $Q_G$. For example, to test a flip-flop, attach the data and control inputs of the device under test (DUT) to the stimulus register ($IC_1$), attach the DUT's outputs to the response register ($IC_2$), and attach the DUT's clock input to signal $\overline{P_1}$ (also called $Q_B$). When you run the SR test with $Q_C$ selected to load the response register, $Q_A$ sets the flip-flop's inputs, $Q_B$ clocks the flip-flop, and $Q_C$ records the result. This method allows you to test devices as deep as six ranks.

The interface shown in **Fig 6** is a step-and-record "front panel" for an 8085 CPU. Using the processor's wait line, the interface single-steps the system through 16 or 32 instructions and records the condition of the data, address, and control lines at each step. You can then display the resulting data and trace the program flow. The drivers and registers, $IC_1$ through $IC_6$, interface and multiplex the CPU signals on $P_{101}$ to the response port of the test computer. The remaining ICs, $IC_7$ through $IC_{12}$, control the interface and the CPU. Port C of the test computer controls operation of the interface. **Table 1** shows the assignment of the port C bits.

**TABLE 1—PORT C BIT ASSIGNMENT**

| | | |
|---|---|---|
| PC0 | AUTO MODE | HIGH TO ENABLE AUTOMATIC STEPPING |
| PC1 | *RUN/STOP | LOW TO RUN CPU, HIGH TO STOP |
| PC2 | *FULL/HALF | LOW FOR 32 STEPS/CYCLE, HIGH FOR 16 |
| PC3 | NOT USED | |
| PC4 | RESET | RESETS THE CPU WHEN LOW |
| PC5 | STEP | STEPS THE CPU ONE MEMORY CYCLE WHEN HIGH |
| PC6, 7 | NOT USED | |

To operate the interface, send a value of 03 for 32 steps per test or 07 for 16 steps per test to Port C and run an SR test using the incremental data set. In the test, the interface scans the processor signals and stores the result in the response RAM. Then the CPU steps once, and the test repeats. When the test is completed, you can use the monitor to dump the response data to the screen. The resulting data are shown in **Table 2**.

**TABLE 2—INTERPRETATION OF MONITOR DISPLAY**

XXXX AH AL DD SS CC II 00 00. . . ,
WHERE
XXXX IS THE RESPONSE RAM ADDRESS,
AH IS THE CPU HIGH ADDRESS BYTE,
AL IS THE CPU LOW ADDRESS BYTE,
DD IS THE CPU DATA BYTE,
SS IS THE CPU STATUS,
CC IS THE CPU CONTROL STATE, AND
II IS THE CPU INTERRUPT STATE.

Because the monitor prints 16 RAM data values per line and the test reports eight bits per step, the second half of the line includes all zeros for a 16-step test. For a 32-step test, the second half of the line contains the next step's data set. After you evaluate the data, run the SR command again for the next 16 or 32 steps. You can repeat this process as many times as required.

Note that the interface inserts long wait states into

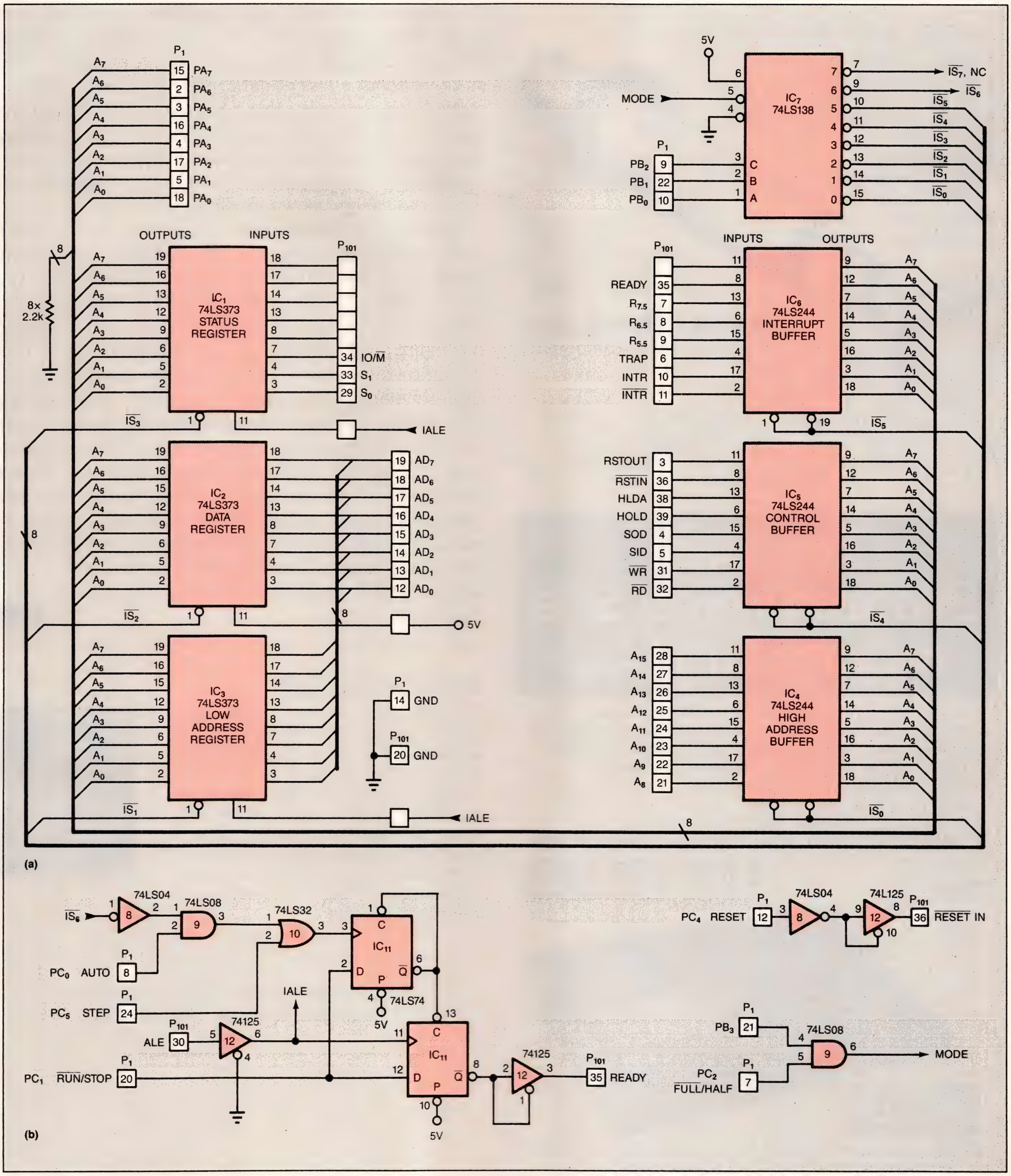
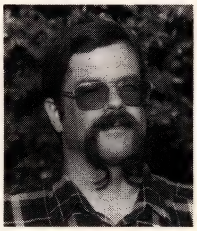



*Fig 6—The CPU front panel* consists of a data multiplexer *(a)*, a wait-state generator *(b)*, and control logic.

the program execution and therefore extends the program timing significantly. In addition, many systems that use dynamic RAM won't allow extended wait states without a loss of data. For a small system using static RAM, however, this interface is ideal for tracing the program flow. You can easily design an interface for almost any type of processor because you only need to change the wait generator and the interconnect wiring in the design shown in **Fig 6.**

As the preceding examples illustrate, you can use a small microcomputer as an SR system to run many useful tests. In addition to the units described, you can construct interfaces for many other functions. For example, if you add an analog-to-digital converter to the input of an interface and a digital-to-analog converter to the output, you can create a waveform recorder/generator. Because the monitor—including the SR command routines—requires only 2k bytes of memory, the system can also include many other test functions. Using the interfaces described in the various examples and the appropriate routines, you can test serial and parallel interfaces, convert serial signals to parallel signals and vice versa, generate square waves and digital patterns, scan lines that carry digital signals and print their logic states, and operate several other interfaces. **EDN**

## Author's biography



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# Use a logic analyzer to debug real-time software

*Cleaning up real-time operating bugs requires real-time monitoring and analysis, for which the best tool is still the logic analyzer. However, to use a logic analyzer effectively, you need to understand the special triggering requirements that multiprocessing presents.*

Ken Marti, *Tektronix Inc*

The logic analyzer is a valuable tool not only for debugging hardware, but also for monitoring and debugging real-time software that runs on microprocessor-based systems. Although you can perform the initial stages of the debugging process by running software debuggers on the development system, certain problems remain hidden until you test the software in real time on the target system. A logic analyzer provides the best method of monitoring this complex stage of the debugging process. By examining the nature of the real-time operating problems, you can determine which capabilities to look for in a logic anlayzer.

It's relatively easy to use a logic analyzer to debug small, ROM-based systems because the code is always resident in memory at fixed addresses. Large systems that use multiprocessing, time-sharing methods, on the other hand, are more challenging to debug. Typical multitasking systems run the operating-system kernel (or supervisor) and the user processes. The kernel is located in a fixed area of memory and is therefore easy to monitor with a logic analyzer. The user processes, however, aren't permanently resident in memory and don't always occupy the same area of memory when they are active. The multitasking computer loads and runs user processes dynamically; that is, it loads the code into whatever areas of memory are currently available. You don't have to abandon your monitoring procedures just because user processes are transient; a logic analyzer can help you overcome the process-identification problem by detecting complex triggering conditions.

To understand how you can apply a logic analyzer to real-time software debugging, consider the life of a user process. **Fig 1** shows the sequence of events of a typical user process, Process A.

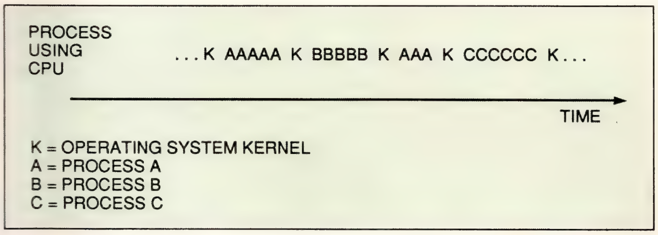


***Fig 1—The operating system kernel controls the order** in which user processes run, and assigns time slices and resources to each process.*

*To debug a multiprocessing system, you must be able to monitor and analyze data flow and control events in real time. A logic analyzer gives you that ability.*

- The occurrence of some event requires the execution of Process A.
- The kernel fetches Process A into memory from disk storage.
- The kernel causes Process A to begin executing.
- Process A runs until it completes its task and exits, or until the kernel suspends the process. The kernel may suspend Process A for several reasons. For example, if the process uses all of its time slice without completing its task, the kernel gives another user process a chance to run. Or, if Process A requires a system resource that is temporarily unavailable, the kernel notes the request and suspends the process until the resource becomes available.
- Eventually, the kernel reactivates Process A, which runs until it either exits or is suspended again by the kernel.

The multiple user processes run in discrete time-slice assignments, which the kernel assigns. The kernel runs in the intervals between each user time slice and, during these periods, allocates any system resources that the user processes need.

In systems that don't have a memory management unit (MMU) or in systems that have an MMU that is outside of the CPU chip, all user processes usually start at the same logical address (often address 0). Before executing a user process, the kernel must set up the MMU (or some other address-conversion device) so the process will address the appropriate area of physical memory (**Fig 2**).

Because all user processes start at the same logical address, you can't use addresses to distinguish among user processes. If, for example, you set up the logic analyzer to trigger on address 7000 in the user-program space, the logic analyzer triggers on *any* user process that accesses address 7000. To identify the user processes, you need a way of telling the logic analyzer how to recognize when Process A is running and when it isn't running. Your logic analyzer must be able to examine only Process A and ignore activities that take place when Process A is not running.

If you know how to tell when Process A is running, you can set up a logic analyzer to trigger on an event rather than on an address. The state diagram in **Fig 3** is a simple example of this triggering concept.

In the setup shown in **Fig 3,** the logic analyzer's control logic stays in State 1 and looks only for the event (in the kernel) that indicates that Process A is about to run. When the logic analyzer recognizes such an event, the control logic advances to State 2. In State 2, the control logic looks for Event 1, and, if the event occurs, it triggers the logic analyzer. The control logic remains in State 2 until an event (again, in the kernel) indicates that Process A is being suspended or is exiting. The control logic then returns to State 1.

In a more realistic case, you may want to trigger on a sequence of events occurring in Process A. For example, you can trigger on the completion of the sequence "Event 1, followed by Event 2, followed by Event 3." You may be tempted to use a simple approach such as the one illustrated in **Fig 4;** however,

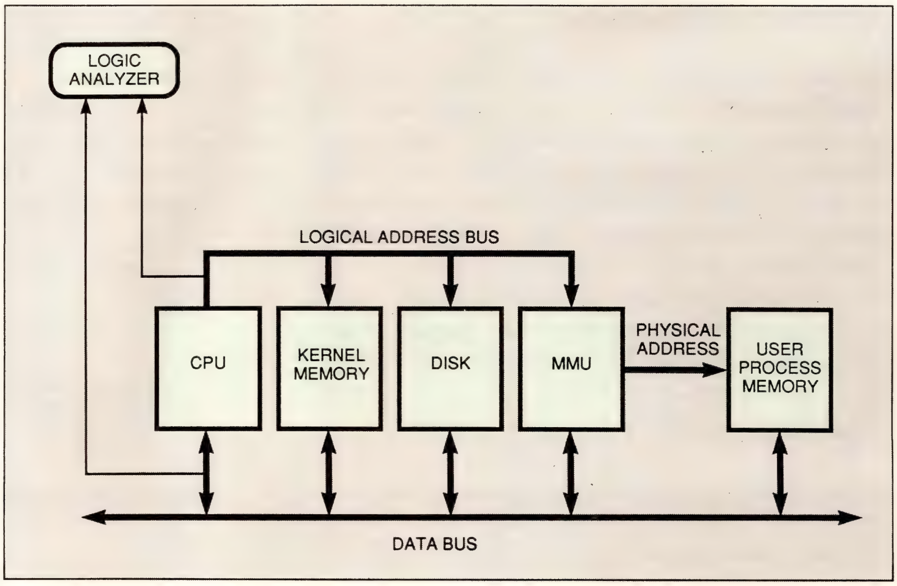


***Fig 2—To monitor a memory-managed, μP-based system,*** *a logic analyzer needs access to the logical address at the CPU pins and access to the data pins.*

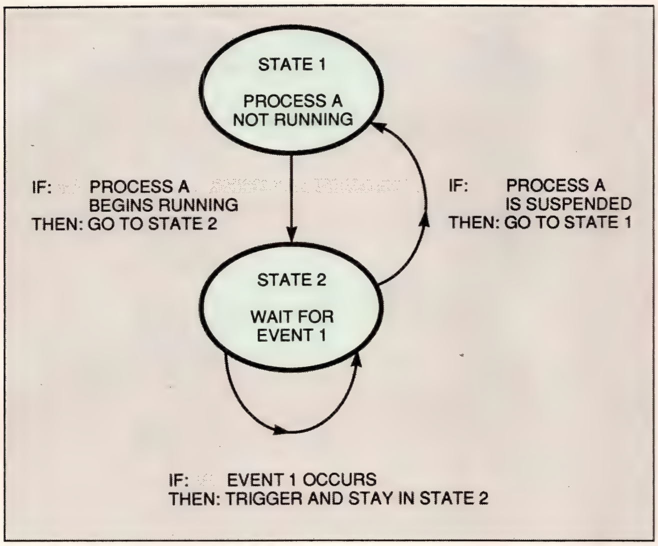


***Fig 3—This state diagram of a logic-analyzer program*** *shows the conditions for triggering the analyzer on EVENT 1 in Process A and for ignoring all other processes.*

such a state machine won't work in this application. Any suspension of the process after Event 1 but before Event 3 returns the state machine to State 1; the state machine doesn't recognize the sequence unless all three events occur within a single time slice.

To detect a sequence of events in Process A when suspensions may occur, you need a state machine with the following capabilities:

- Each state must recognize when Process A is suspended.
- In case the kernel suspends Process A during the event sequence, each state must always remember the occurrence of the event with which it is currently associated. When the kernel reactivates Process A, control can then return to the correct state.

The state diagram in **Fig 5** shows you how to add these capabilities to your state machine. The modified state machine detects the sequence "Event 1, Event 2, and Event 3"—even if the process is suspended between individual events in the sequence. The state machine triggers the logic analyzer only when the event sequence is completed.

To apply the complex triggering functions shown in **Fig 5**, you need a logic analyzer with more capabilities than the basic feature set. First, you need a logic analyzer with a trigger mechanism that is implemented as a state machine. The more states an analyzer can store, the larger the sequence of events it can recognize. Second, the trigger mechanism must be able to detect the occurrence of each independent event within each state. Finally, the trigger mechanism must have several word recognizers and a way to record its progress through the sequence of events. In **Fig 5,** for example, the flags track the trigger mechanism's progress.

Using a logic analyzer that has these capabilities, you can easily create a multievent triggering program. The sample program in **Table 1** is one specific example, which causes triggering on the sequence "Event 1, Event 2, Event 3." It is designed for use on a Tektronix DAS 9200 logic-analyzer system that includes a 92A60

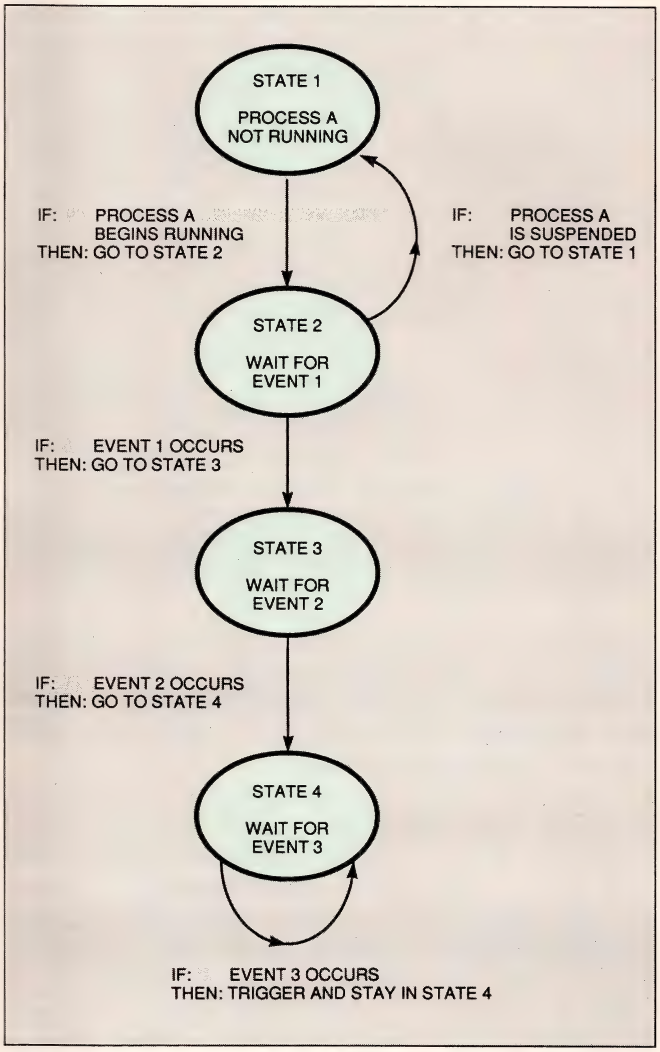


***Fig 4—You can set up complex, multievent triggering*** *by recognizing the sequence EVENT 1, EVENT 2, EVENT 3, in Process A. However, this particular approach does not recognize the temporary suspension of Process A during the sequence.*

*Because all processes start at the same address (unless the CPU has a built-in MMU), you can't distinguish between processes on the basis of address alone.*

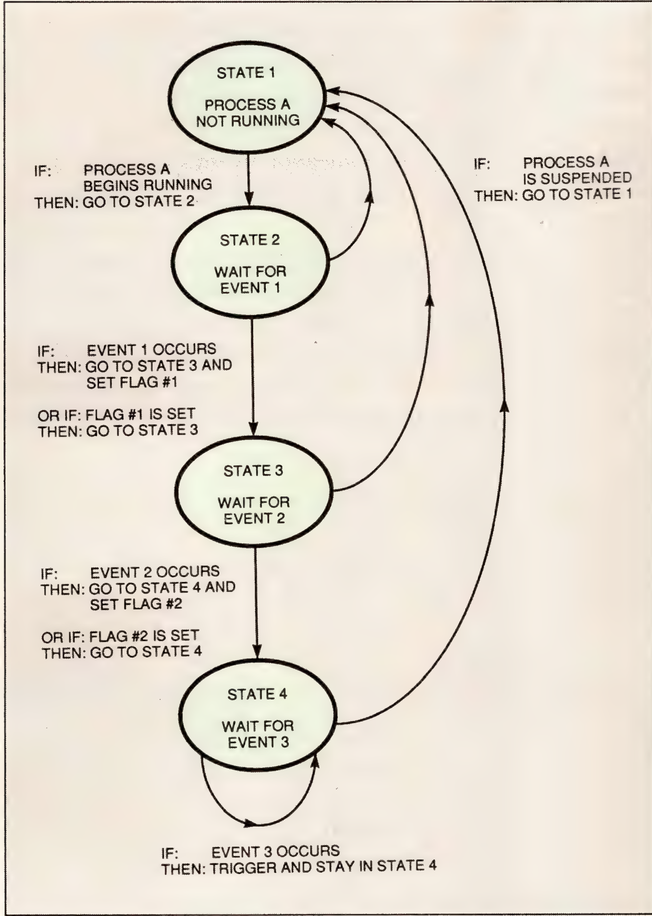


***Fig 5—An effective multievent triggering method*** *stores the occurrence of each event in the triggering sequence. It also recognizes suspension of Process A at any time in the event sequence and returns to the correct state when the kernel reactivates Process A.*

**TABLE 1—SAMPLE ANALYZER PROGRAM FOR 3-EVENT SEQUENCE**

| | | | |
|---|---|---|---|
| STATE WAIT_PROC_A | IF WORD #1= | ADDRESS: | CURRENT PROCESS |
| | | DATA: | PROCESS A |
| | | CONTROL: | SUPER_DATA |
| | THEN | GOTO STATE | WAIT_EVENT_1 |
| STATE WAIT_EVENT_1 | IF WORD #2= | ADDRESS: | CURRENT PROCESS |
| | | DATA: | DON'T CARE |
| | | CONTROL: | SUPER_DATA |
| | AND WORD #3 != | ADDRESS: | DON'T CARE |
| | | DATA: | PROCESS A |
| | | CONTROL: | DON'T CARE |
| | THEN | GOTO | STATE WAIT_PROC_A |
| | OR IF WORD #4= | ADDRESS: | EVENT 1 |
| | | DATA: | DON'T CARE |
| | | CONTROL: | USER_PROG |
| | THEN | SET | FLAG #1 |
| | OR IF FLAG #1 | IS SET | |
| | THEN | GOTO | STATE WAIT_EVENT_2 |
| STATE WAIT_EVENT_2 | IF WORD #2= | ADDRESS: | CURRENT PROCESS |
| | | DATA: | DON'T CARE |
| | | CONTROL: | SUPER_DATA |
| | AND WORD #3 != | ADDRESS: | DON'T CARE |
| | | DATA: | PROCESS A |
| | | CONTROL: | DON'T CARE |
| | THEN | GOTO | STATE WAIT_PROC_A |
| | OR IF WORD #5= | ADDRESS: | EVENT 2 |
| | | DATA: | DON'T CARE |
| | | CONTROL: | USER_PROG |
| | THEN | SET | FLAG #2 |
| | OR IF FLAG #2 | IS SET | |
| | THEN | GOTO | STATE WAIT_EVENT_3 |
| STATE WAIT_EVENT_3 | IF WORD #2= | ADDRESS: | CURRENT PROCESS |
| | | DATA: | DON'T CARE |
| | | CONTROL: | SUPER_DATA |
| | AND WORD #3 != | ADDRESS: | DON'T CARE |
| | | DATA: | PROCESS A |
| | | CONTROL: | DON'T CARE |
| | THEN | GOTO | STATE WAIT_PROC_A |
| | OR IF WORD #6= | ADDRESS: | EVENT 3 |
| | | DATA: | DON'T CARE |
| | | CONTROL: | USER_PROG |
| | THEN | TRIGGER | |

acquisition module. The target system is a Motorola 68010-based system that runs under a proprietary implementation of the Unix operating system. However, you can modify the program for any general-purpose, multitasking operating system.

### A sample trigger program

**Table 1** shows a slightly modified version of what you see on the analyzer screen during the setup process. The analyzer lets you move the cursor to various highlighted fields to define states. For some fields, such as the word number, a pop-up menu lets you select "=" or "!=." You then enter symbols or hexadecimal numbers to define the Address, Data, and Control values.

The DAS 92A60 trigger program consists of four states: Wait_Proc_A, Wait_Event_1, Wait_Event_2, and Wait_Event_3. Only one of these states is active at a given time. Each state contains a variable number of clauses in the form "IF event(s) . . . THEN action(s)." When a state becomes active, the control logic evaluates each clause in that state and executes the actions associated with any events that are true. A 'Go To State' action sets the state machine to a different state.

The sample program breaks each word into three groups. The Address group always specifies the memory address currently being accessed. The Data group

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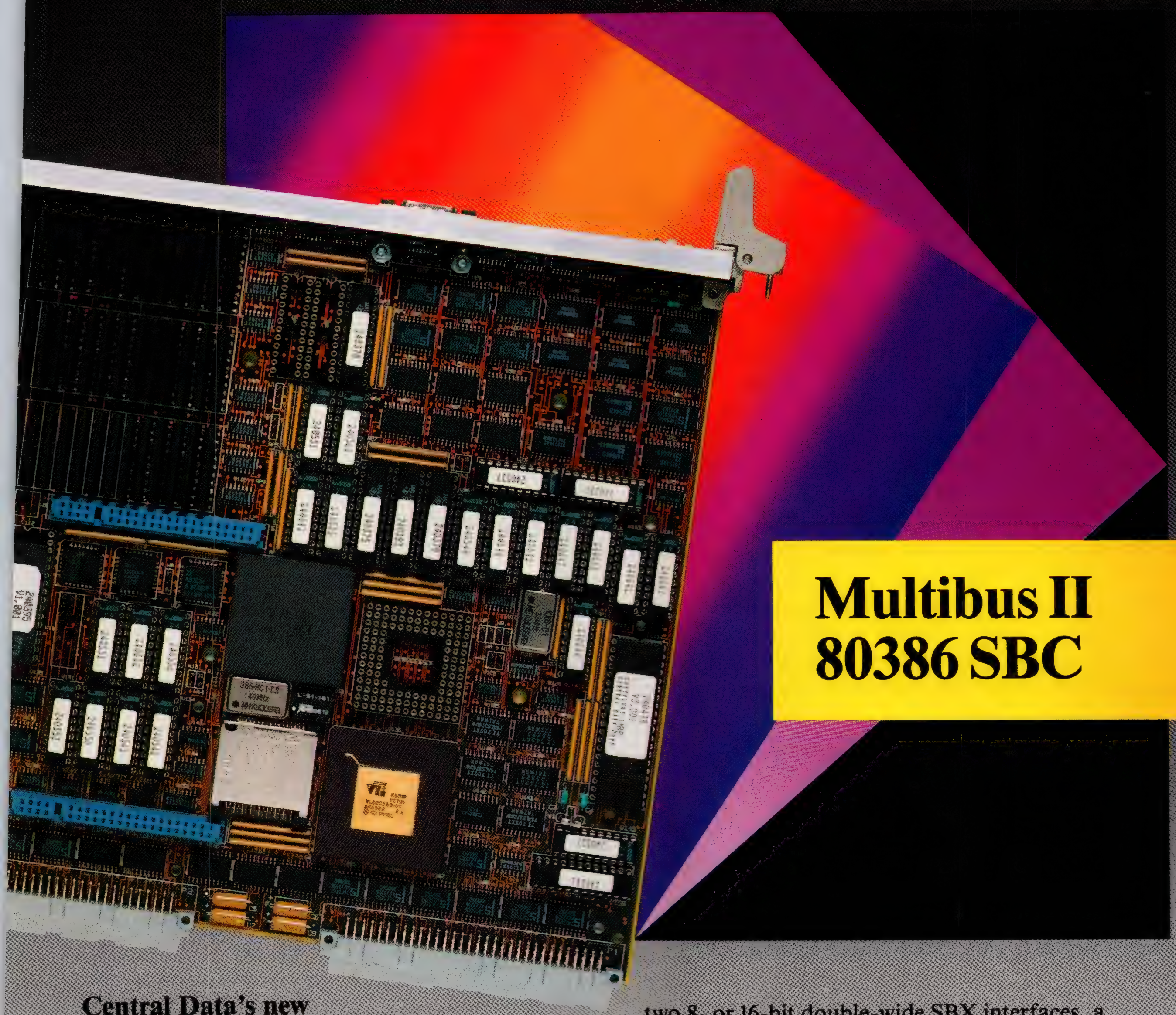


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specifies the data being written to the address. The Control group specifies whether the kernel (SUPER_DATA) or a user program (USER_PROG) is performing the read or write.

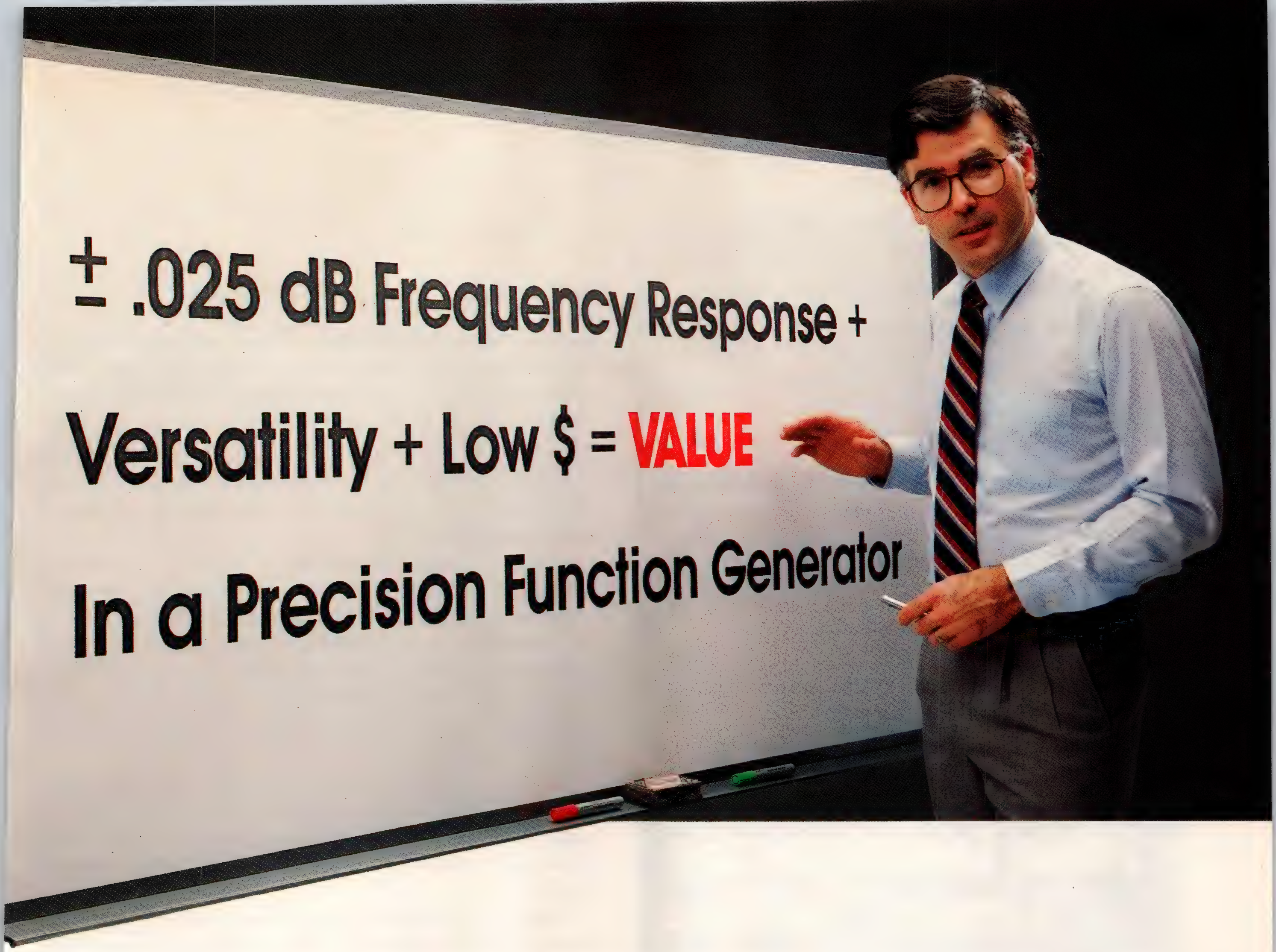
To specify the values that the state machine must recognize, the program uses symbolic names rather than binary or hexadecimal numbers. **Table 2** shows the format of the corresponding symbol tables. The Address and Data groups contain only the items that you define in your program and their hexadecimal equivalents. The Control group shows the names and the binary equivalents of all types of bus operations that the control logic can recognize for the microprocessor. The highlighted areas indicate the three items that are relevant to the sample program.

When you start the logic analyzer, or when the kernel reactivates Process A after a suspension, State 1 (Wait_Proc_A) becomes active. Wait_Proc_A contains only one clause, which waits for an event to indicate that Process A is about to be executed. In the sample program, for example, the clause waits for the kernel to write Process A's identifier (ID), PROCESS A, into CURRENT PROCESS, which is a memory location in the kernel's data space. CURRENT PROCESS always contains the ID of the current user process. State 2 (Wait_Event_1) then becomes the active state.

State 2 (Wait_Event_1) contains three clauses. The first clause watches for an event that indicates the temporary suspension of PROCESS A. The clause in the sample program recognizes the suspension when the kernel writes a process ID other than PROCESS A to kernel address CURRENT PROCESS. When the suspension occurs, State 1 becomes the active state. The second clause watches for EVENT 1 in Process A. In this example, EVENT 1 is the execution of a routine beginning at the user address 01D5C6. If EVENT 1 occurs, the control logic sets Flag #1, which,

## TABLE 2—LOGIC ANALYZER SYMBOL TABLES

| ADDRESS GROUP | | DATA GROUP | | CONTROL GROUP | |
|---|---|---|---|---|---|
| CURRENT PROCESS | 040E3E | PROCESS A | 003C | SYSTEM_RESET | XX XXXX 00XX XXXX |
| EVENT 1 | 01D5C6 | DON'T CARE | XXXX | PREFETCH? | 00 1X10 XXXX X111 |
| EVENT 2 | 01CFDE | | | AUTOVECTOR | XX 1111 XXXX XX0X |
| EVENT 3 | 01EB76 | | | SPURIOUS_INT | XX 1111 XXXX X0XX |
| DON'T CARE | XXXXXX | | | INT_ACK | X1 1111 XXXX XXXX |
| | | | | DMA_READ | XX 1XXX XXXX XXX0 |
| | | | | DMA_WRITE | XX 0XXX XXXX XXX0 |
| | | | | DMA | XX XXXX XXXX XXX0 |
| | | | | INVALID_DMA | 11 XXXX XXXX XXX0 |
| | | | | RESET | XX XXXX X0XX XXXX |
| | | | | HALT | XX XXXX 0XXX XXXX |
| | | | | BUS_REQUEST | XX XXXX XXXX 0XXX |
| | | | | BUS_GRANT | XX XXXX XXX0 XXXX |
| | | | | BUS_ERROR | XX XXXX XXXX X0XX |
| | | | | B_ERR_RETRY | XX XXXX 0XXX X0XX |
| | | | | VMA | XX XXXX XXXX XX0X |
| | | | | DATA_SPACE_RD | XX 1X01 XXXX XXX1 |
| | | | | DATA_SPACE_WR | XX 0X01 XXXX XXX1 |
| | | | | READ | 00 1XXX XXXX XXXX |
| | | | | READ_L | 10 1XXX XXXX XXXX |
| | | | | READ_U | 01 1XXX XXXX XXXX |
| | | | | READ_ANY | XX 1XXX XXXX XXXX |
| | | | | WRITE | 00 0XXX XXXX XXXX |
| | | | | WRITE_L | 10 0XXX XXXX XXXX |
| | | | | WRITE_U | 01 0XXX XXXX XXXX |
| | | | | WRITE_ANY | XX 0XXX XXXX XXXX |
| | | | | **SUPER_DATA** | **XX X101 XXXX XXXX** |
| | | | | SUPER_PROG | XX X110 XXXX XXXX |
| | | | | SUPERVISOR | XX X1XX XXXX XXXX |
| | | | | USER_DATA | XX X001 XXXX XXXX |
| | | | | **USER_PROG** | **XX X010 XXXX XXXX** |
| | | | | USER | XX X0XX XXXX XXXX |
| | | | | PROG_SPACE | XX XX10 XXXX XXXX |
| | | | | DATA_SPACE | XX XX01 XXXX XXXX |
| | | | | CPU_SPACE | XX X111 XXXX XXXX |
| | | | | **"DON'T CARE"** | **XX XXXX XXXX XXXX** |

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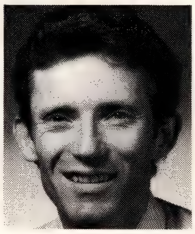
in turn, makes State 3 (Wait_Event_2) the active state in the next cycle. If Flag #1 is already set when State 2 becomes active, the third clause immediately causes State 3 (Wait_Event_2) to become the active state. The third clause is needed so that the state machine can return to the correct state in the trigger program if Process A is suspended at any time before the 3-event sequence ends.

State 3 (Wait_Event_2) is similar to State 2 (Wait_Event_1), except that it watches for the occurrence of EVENT 2 (rather than EVENT 1) in Process A. State 3 passes control to State 4. In the sample program, EVENT 2 is the execution of a routine beginning at user address 01CFDE. Again, if the kernel suspends Process A, state machine returns to State 1 (Wait_Proc_A).

State 4 (Wait_Event_3) has only two basic functions. If EVENT 3 in Process A takes place, the control logic triggers the logic analyzer. On the other hand, any suspension of Process A returns the state machine to State 1.

Clearly, this sample trigger program is designed for a very specific situation. The details of the program are markedly different for each application. However, the program does illustrate the impressive software tracking functions you can perform with a state-of-the-art logic analyzer that is suitable for software debugging. EDN

## Author's biography



*Ken Marti is a senior software engineer at Tektronix Inc (Beaverton, OR), where he has spent 10 years designing and developing application software. Ken holds a BS degree in computer science from Utah State University. In his spare time, Ken enjoys soccer, racquetball, and skiing.*

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LINEAR TECHNOLOGY

# DESIGN NOTES

*Number 21 in a series from Linear Technology Corporation* *April, 1989*

## Floating Input Extends Regulator Capabilities

Brian Huffman

Many applications require circuit performance that is unachievable with conventional regulator design. This results in added complexity to the circuit. However, some problems can easily be solved by floating the input to the regulator. A floating input can either be a battery, or a secondary winding that is galvanically isolated from all other windings. With this method high efficiency negative voltage regulation, high voltage regulation, and low saturation loss positive buck switching regulator can all be achieved easily.

Low dropout negative voltage regulators are not currently available. This would seem to preclude high efficiency negative linear regulators. Such regulation is frequently desired in switching supply post regulators; however, if the secondary windings are isolated from one another, a low dropout positive voltage regulator can be used for negative regulation (Figure 1).

In this circuit the LT1086 servos the voltage between the output and the adjust pin to 1.25V. The positive regulation is accomplished by conventional regulator design. Negative voltage regulation is achieved by connecting the output of the positive voltage regulator to ground. The $V_{IN}$ pin floats to 1.5V or greater, above ground. This technique can be used with any positive voltage regulator, although highest efficiency occurs with low dropout types.

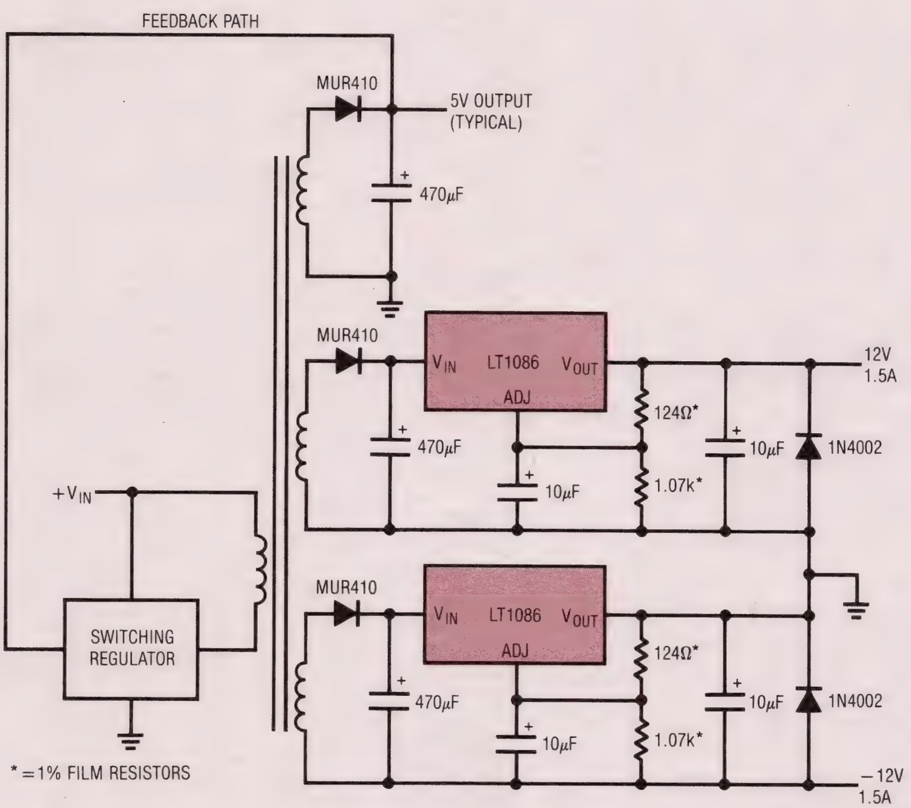


**Figure 1. High Efficiency Negative Voltage Regulation**

Another example where floating a linear regulator can be useful is shown in Figure 2. In this case high voltage regulation can be handled if split secondary windings are available. This allows the regulators to be connected in series. Neither regulator exceeds its maximum differential voltage even under short circuit conditions.

High current positive buck switching regulators can have excessive saturation losses since most switches are Darlingtons. As much as 2V can be dropped across a Darlington or composite PNP switching transistor. However, efficiency can be increased and power dissipation requirements greatly reduced if the input is allowed to float (Figure 3).

The circuit in Figure 3 uses an LT1070 to perform a buck conversion. The LT1070 is a current mode switching regulator. The $V_{SW}$ pin output is a collector of a common emitter NPN, so current flows through it when it is low. The 40kHz repetition rate is set by the LT1070's internal oscillator. When the $V_{SW}$ pin is "on," current flows through the load, the inductor, and into the $V_{SW}$ pin. During this time a magnetic field is built up in the inductor. When the switch in turned "off," the magnetic field collapses dumping energy into the load through D1. The input of the switching regulator floats to a potential set by the output.

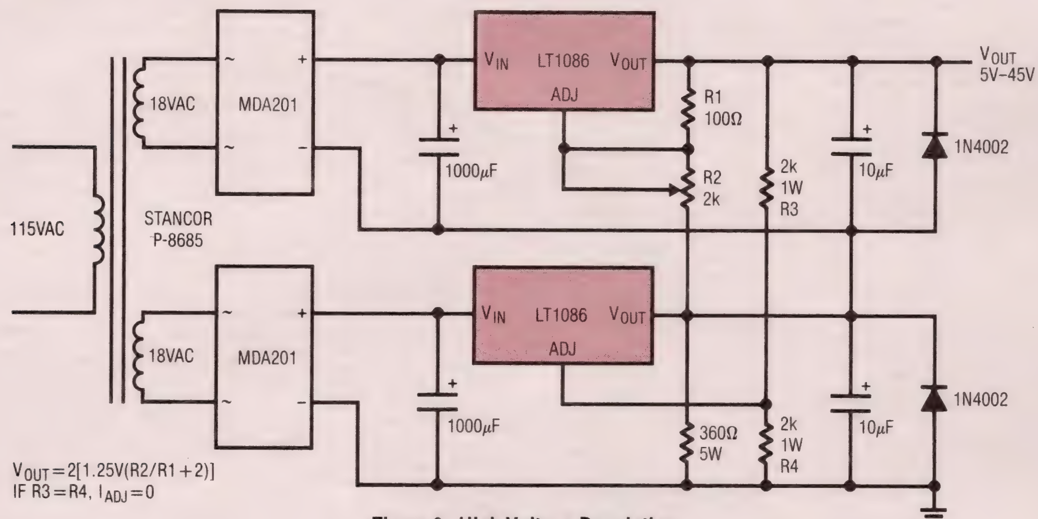


**Figure 2. High Voltage Regulation**

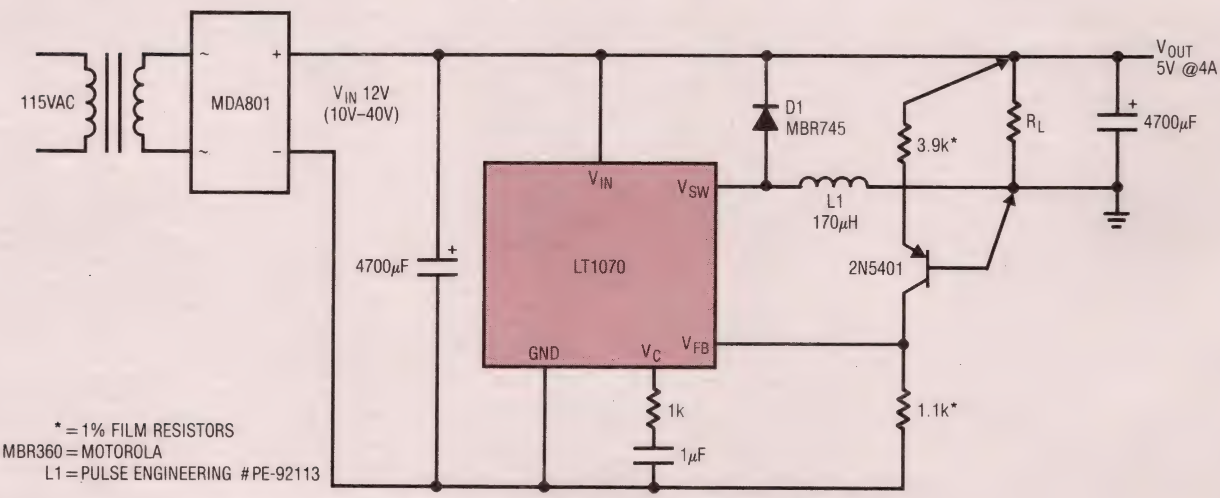


**Figure 3. Floating Input Low Saturation Loss Buck Regulator**

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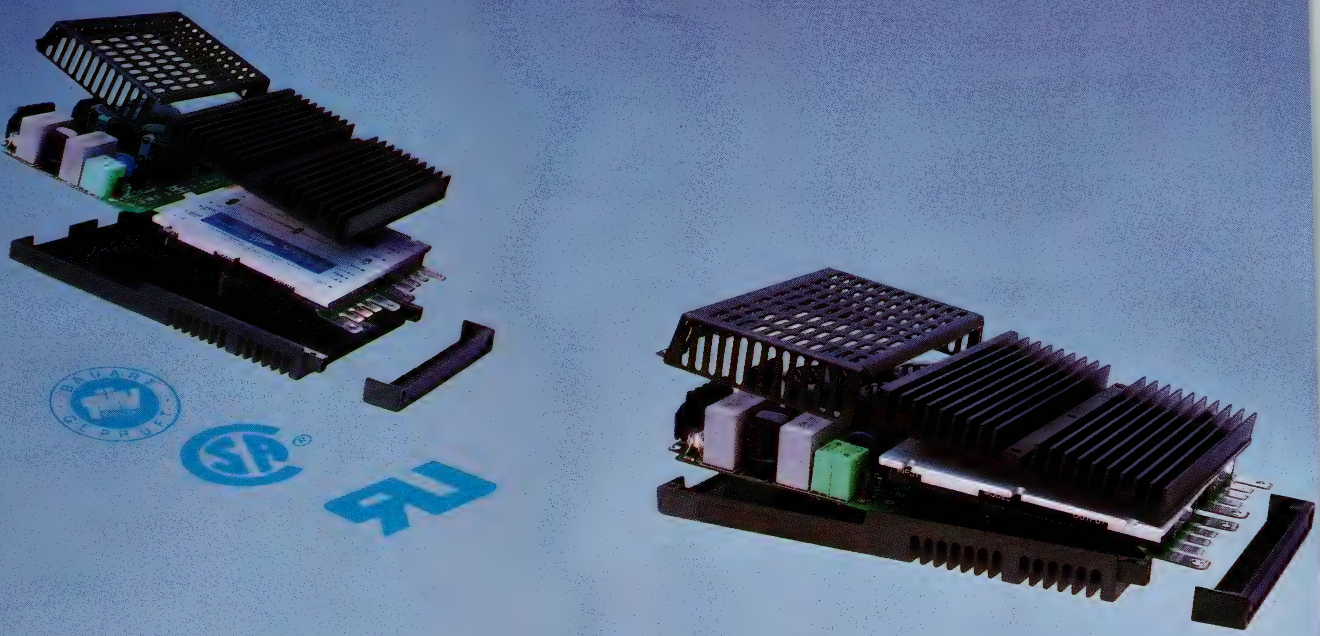

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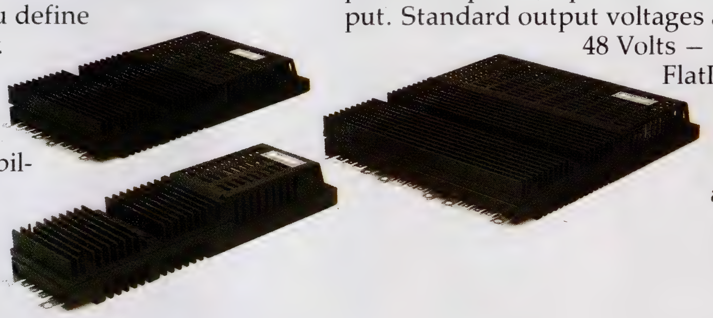

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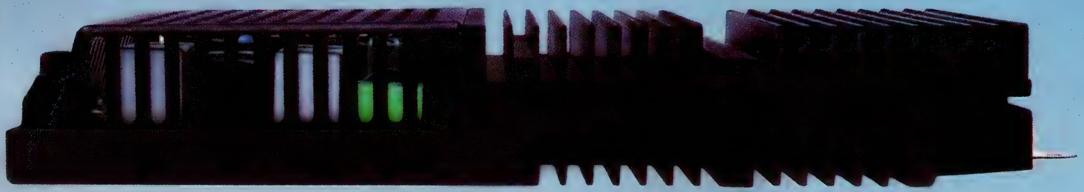

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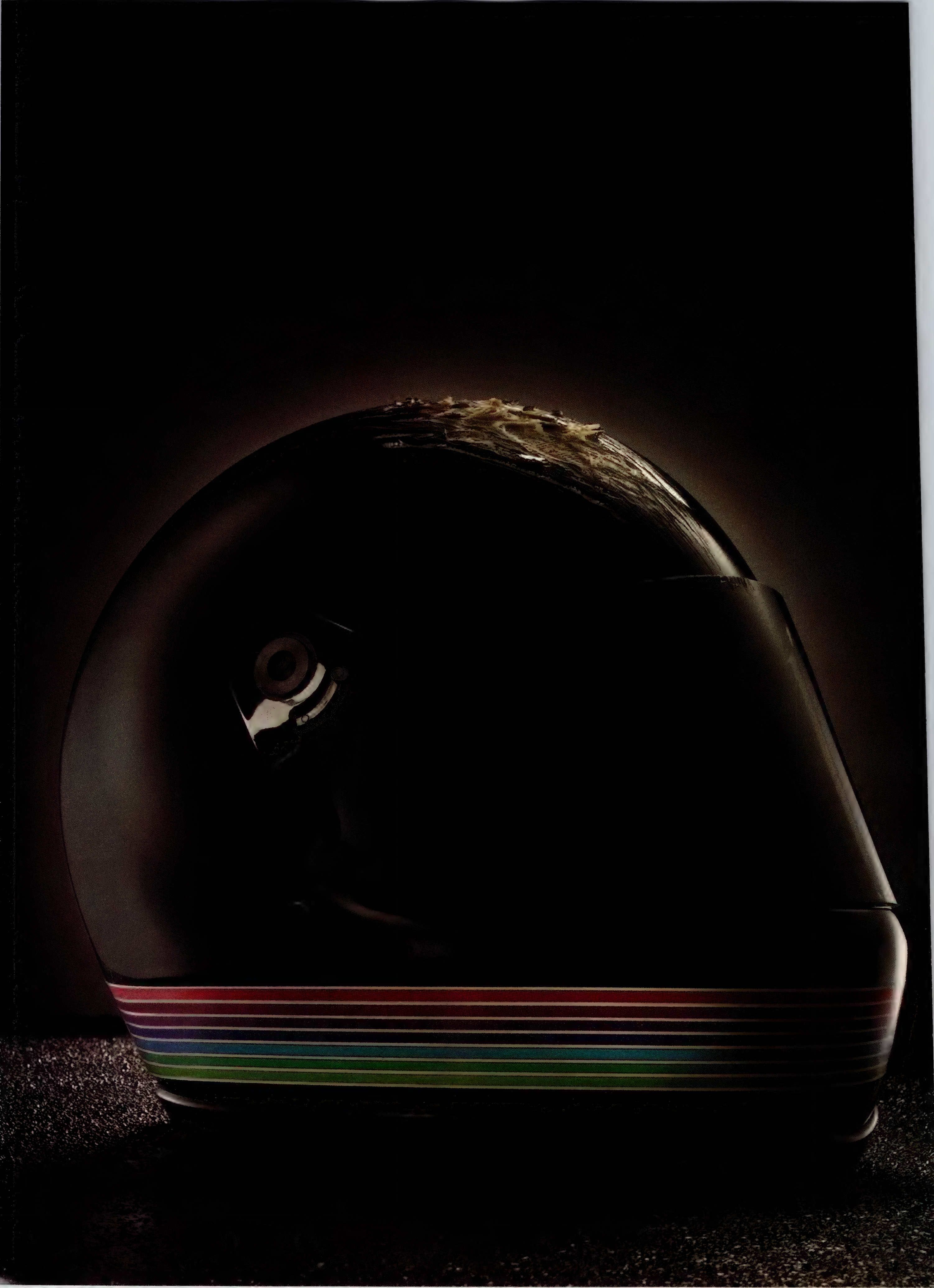

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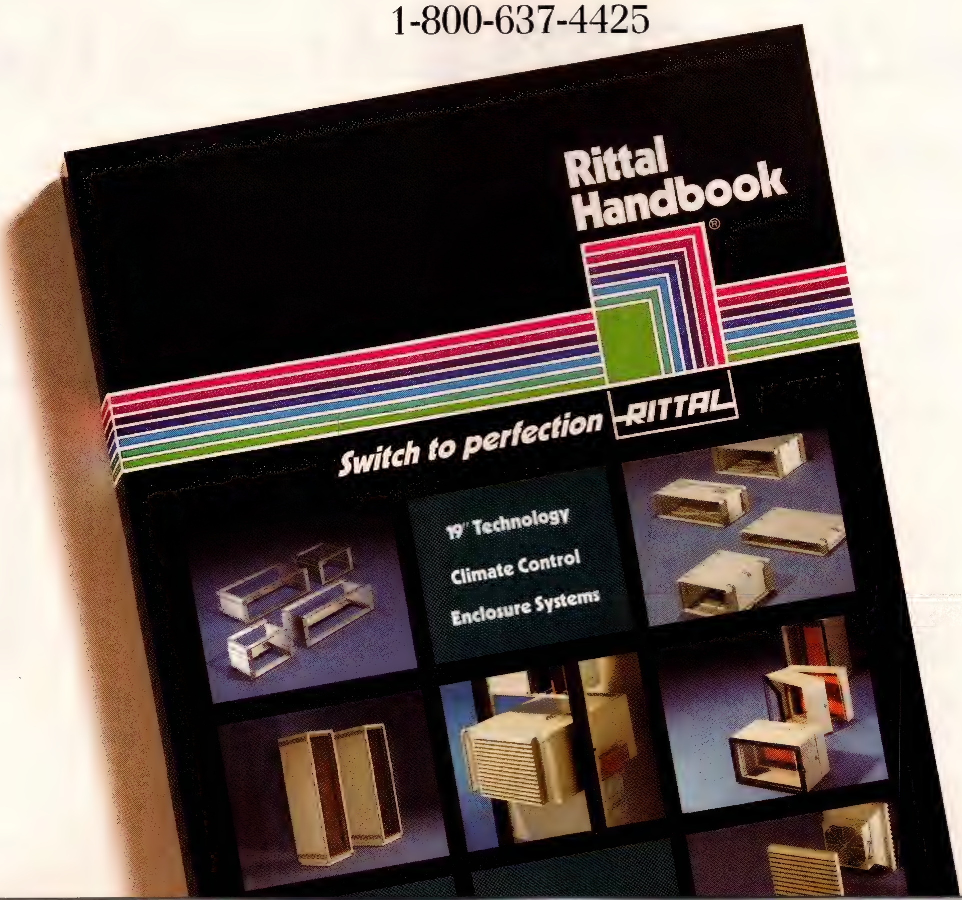


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# NPN replaces PNP pass transistor

Brian Huffman
*Linear Technology Corp, Milpitas, CA*

Classic buck switching regulators and power supplies use PMOS or PNP transistors as their series-pass switch. In general power-supply design, you should use low on-resistance switches to achieve high efficiency and minimize heat sinks. Unfortunately, low on-resistance PMOS transistors just aren't available. The lowest on-resistance PMOS devices available typically have 0.3Ω on-resistances; comparable NMOS devices have 0.028Ω on-resistances.

You can use an NMOS transistor as a series-pass switch if you drive its gate sufficiently higher in voltage than its source, thus causing the transistor to saturate. The circuit in **Fig 1** bootstraps its NMOS transistor's gate off its source to achieve saturation.

In the **figure**, the LT1072 switching-regulator controller sinks current into its $V_{SW}$ input, which is a common-emitter NPN driver, at a 40-kHz repetition rate. When the $V_{SW}$ output is off, the gate of $Q_2$ goes high, causing it to saturate and turn $Q_1$ off. When $Q_1$ turns off, the flying capacitor, $C_1$, charges up through $D_1$.

When the LT1072's $V_{SW}$ pin turns on, $Q_2$ turns off and $Q_3$ turns on. The voltage across the flying capacitor now appears across the gate-source junction of the NMOS transistor, $Q_1$, causing it to saturate.

As is usual for buck converters, while $Q_1$ is on, the inductor $L_1$ charges up. When the $V_{SW}$ pin turns off, the inductor dumps its charge into the load with the aid of the freewheel diode, $D_2$.

The remainder of the auxiliary circuitry provides normal power-supply functions. For example, capacitor $C_3$ slow starts the converter, while the 20Ω resistors reduce voltage spikes that would otherwise be generated by $Q_1$'s fast switching. The regulator's high-impedance error-amplifier input, $V_C$, uses an RC damper for loop compensation.

$Q_4$ through $Q_7$ provide short-circuit protection. The LT1004 voltage reference and $Q_6$ and the 7.5-kΩ resistor generate a 240-mA current. This current flows through $R_1$ and generates a threshold voltage of 240 mV for the comparator formed by $Q_4$ and $Q_5$. When the voltage drop across the 0.018Ω sense resistor exceeds 240 mV, $Q_7$ turns on. The chip's $V_{SW}$ pin goes off when $Q_7$ pulls the VC pin below 0.9V. The RC network, $C_2$ and $R_2$, suppresses line transients that might prematurely turn on $Q_7$. EDN

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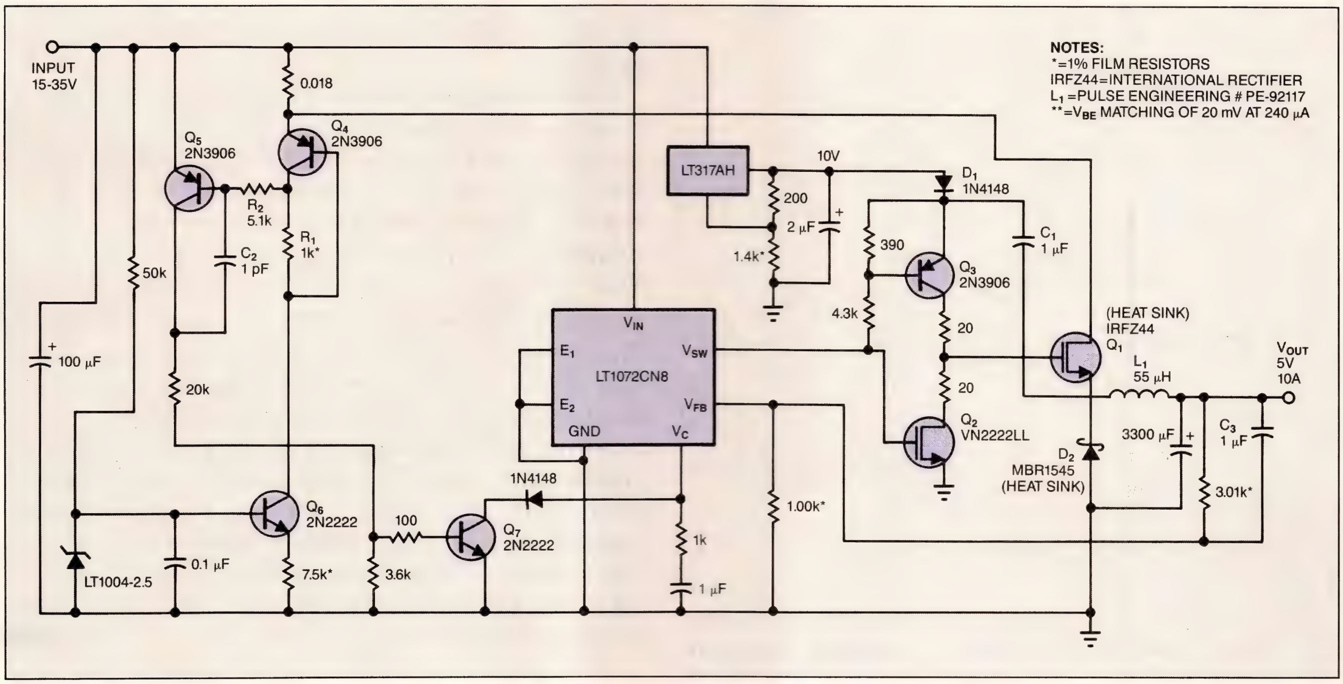


*Fig 1—A bootstrapped, flying capacitor, $C_1$, enables this switching regulator to use a low on-resistance, NMOS series-pass switch instead of a conventional PMOS or PNP device.*

# Variable slew-rate filter tames noise

Jonathan Audy
*Precision Monolithics Inc, Santa Clara, CA*

The variable slew-rate filter in **Fig 1** reduces the noise of an input signal by using a combination of linear and nonlinear filtering. Under certain input conditions, the circuit acts as a nonlinear, variable slew-rate filter. The circuit's slew rate can vary from volts per second to volts per microsecond.

To understand the difference between a linear filter and a variable slew-rate filter, consider that the corner frequency of a linear filter does not change with varying magnitudes of input-signal level and does not distort the input signal. In contrast, the corner frequency of a nonlinear filter varies inversely with the magnitude of the input signal such that the filter's bandwidth is smaller for larger input signals. As the input signal's frequency approaches the nonlinear filter's corner frequency, no phase delay or attenuation occurs at all. But past this point, the filter severely distorts the input waveform's shape to that of a triangular waveform.

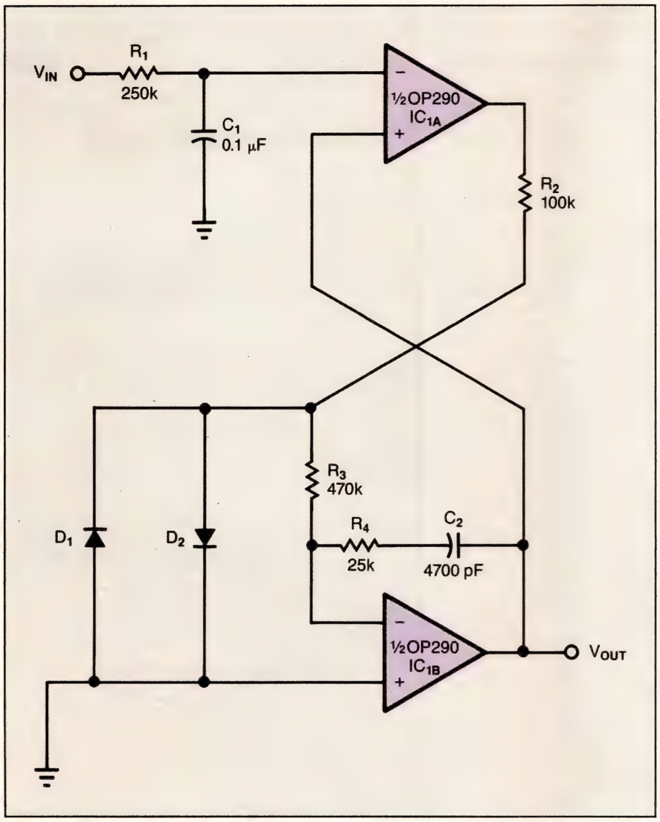


***Fig 1—When input signals are high in magnitude,** this circuit acts as a comparator feeding an integrator to limit the slew rate of the circuit's output. For lower-level inputs, the circuit is simply a unity-gain buffer.*

**Fig 2** shows the circuit's responses to a family of step-input signals having magnitudes from 2 to 12V. The figure demonstrates how the filtering varies from purely linear to a combination of both linear and nonlinear to nonlinear (slew-limiting), depending on the input-step size.

For example, suppose you must handle the ±12V output of a transducer with a circuit whose 90% response time needs to be no faster than 0.1 sec. The problem with using a linear, "capacitor-resistor" type filter to set the response rate of the transducer amplifier is that the rate of change of such a circuit's output increases with increasing input-step size. Therefore, a large noise pulse of short duration would affect the output of a linear filter much more than the output of a nonlinear filter. **Fig 3** shows the response of linear and nonlinear filters to a 12V, 25-msec pulse. Without slew limiting, the output reaches a peak of 8.7V; with slew limiting, the peak reaches 4.4V.

For lower-level inputs, $IC_{1A}$ acts as a gain stage; for larger signals, it functions as a comparator driving an integrator ($IC_{1B}$). Here, the $IC_{1A}$ compares the input voltage to the output voltage of the integrator and forces the integrator's output to equal the input voltage. $IC_{1A}$ needs no feedback resistor because the OP290 op amp is perfectly stable with the feedback provided by $IC_{1B}$.

When the circuit is slew limiting, $IC_{1A}$'s output goes to one of the output rails and the diodes, $D_1$ and $D_2$, clamp the voltage across $R_3$. Thus, a constant current flows into or out of $C_1$. The final result is that $R_3$, $C_2$, and $IC_{1B}$ form an integrator with the output of $IC_{1B}$ slewing at the rate of $V_{DIODE}/(R_3 \times C_2)$ V/sec. For an input voltage that slews at less than this rate, the output of $IC_{1B}$ simply follows the input voltage and $IC_{1A}$ operates linearly with a very high gain. The dc gain of the complete circuit is unity. For non-slewing, dc conditions, the output of $IC_{1A}$ is at 0V.

During slew limiting, one of the diodes carries approximately $V_{SUPPLY}/R_2$, and the other is reverse biased. For the given circuit, $V_{SUPPLY}/R_2 = 15V/100k\Omega = 150\ \mu A$, which yields a diode voltage of 0.3V. The circuit in **Fig 1** has a slew rate of $0.3V/(470\ k\Omega \times 4700\ pF) = 0.136$ V/msec. You can vary this rate by adjusting $R_3$.

EDN

**To Vote For This Design, Circle No 747**

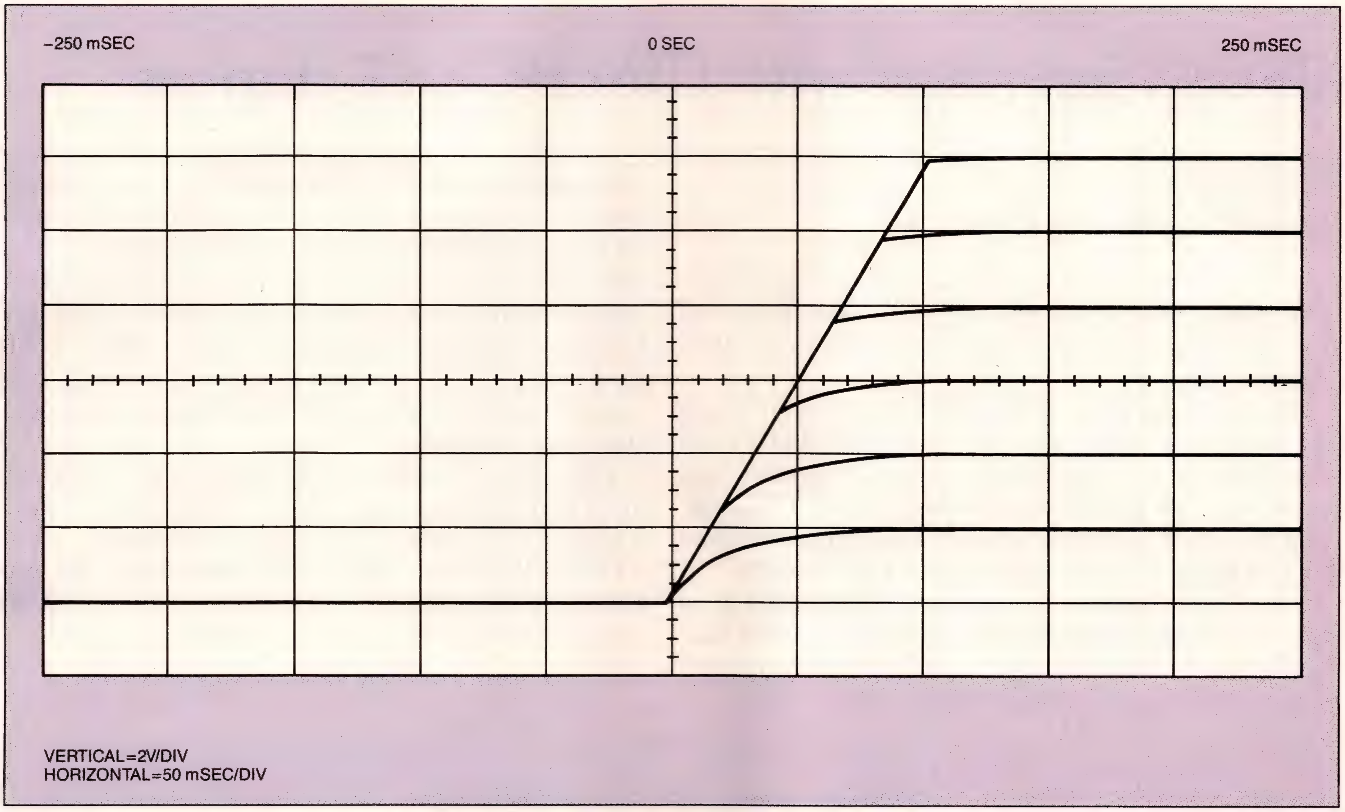


***Fig 2—The responses of the circuit in Fig 1 to a family of*** *step-input signals having magnitudes from 2 to 12V demonstrate how the circuit's filtering varies from purely linear to nonlinear (slew-limiting), depending on the input signal's step size.*

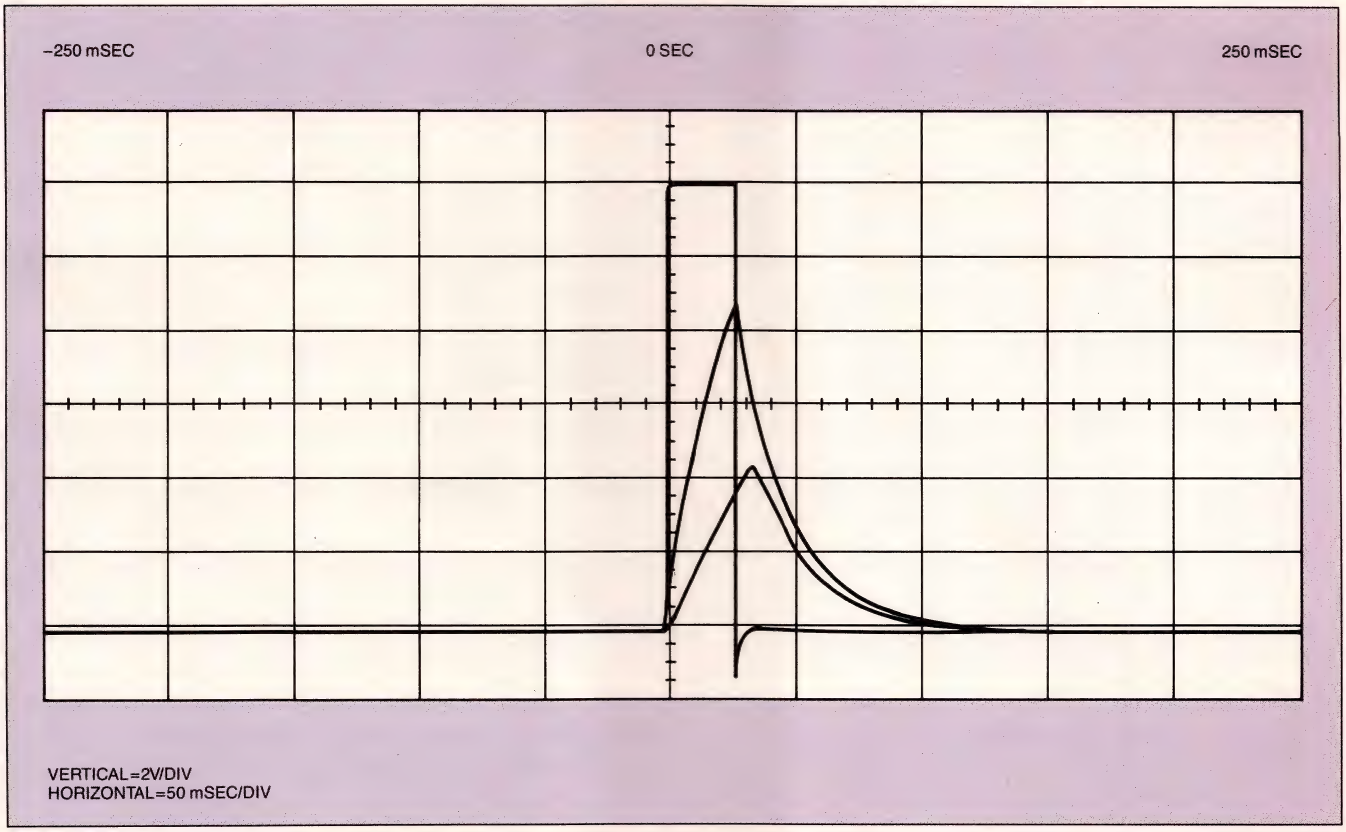


***Fig 3—The slew-rate limiting filter responds much less*** *to a 12V, 25-msec pulse than does a simple RC filter.*

# 386SX interfaces with IBM PC/AT chip set

Al Weidner
*VLSI Technology Inc, Tempe, AZ*

The Intel 80386SX is a 16-bit-bus version of the 32-bit-bus 80386. You can use this µP in an IBM PC/AT to run 386 programs if you adapt the 386SX to the PC's requirements.

The processor clock of the 386SX is 180° out of phase with the clock supplied to the 286 by the IBM PC/AT bus (**Fig 1**). The 74F04 inverter, $IC_2$, corrects this condition. The control lines needed in the PC/AT system to control the status and I/O functions differ from those supplied by the 386SX. The PAL16R6-12, $IC_3$, accomplishes the necessary conversion. **Listing 1** gives the thoroughly tested Boolean equations for the PAL device. Each equation's comments describe the conversion that the equation implements.

Because the 386SX will be operating in its pipelined mode in order to achieve its maximum performance, its address lines will become valid sooner and remain valid for a shorter period than the IBM PC/AT specification requires. To guarantee the correct worst-case timing-specification performance of the IBM PC/AT, three 74LS373 octal latches—$IC_4$, $IC_5$, and $IC_6$—hold the valid address values long enough to ensure recognition by the system.

This adapter handles all available speed variations of VLSI Technology Inc's VL82CPCAT-12QC, VL82CPCAT-16QC, VL82CPCPM-16QC, and VL82CPCPM-20QC IBM PC/AT-compatible chip sets for the 386SX µP. EDN

**To Vote For This Design, Circle No 750**

## LISTING 1—PAL-DEVICE EQUATIONS

```
CHIP     P9TO286            PAL16R6
;PIN#  1     2       3     4     5     6      7     8       9     10
     CLK2  MIO3    WRT3  CMD3  /ADS  /RDY286 /BHE3 RST286  NC    GND
;PIN# 11    12      13    14    15     16     17    18      19    20
     /OE  /BHE2   /SFAZ1 /S0   /S1    MIO    ADS2  SYSCLK RST386 VCC



EQUATIONS
/ADS2 := /(ADS*/ADS2)                  ;2ND PHASE OF ADS, WHETHER READY OR NOT

BHE2  = BHE3*ADS2 + BHE2*/ADS2         ;LATCHED /BHE

SFAZ1:= ADS2*RDY286                    ;1ST STAT PHASE, ALWAYS FOLLOWS ADS
                                       ; WHEN READY

/SYSCLK := SYSCLK + SFAZ1              ;INTERAL SYSCLK - SYNC EACH STATUS CYC.

/RST386 = /(RST286 + RST386*RST286     ;RESET TO TURN OFF ONLY DURING PHASE 2
        +   RST386*SYSCLK)

/MIO := /((ADS*MIO3)+(/ADS*MIO))       ;286 MIO, LATCHED AT EACH ADS PHASE 2

S1    := ADS2*RDY286*/WRT3             ;286  S1, HELD FOR 2 PHASE STAT CYCLE
       + ADS2*RDY286*/CMD3*MIO3        ; 0 ALL OTHER TIMES
       + SFAZ1*S1

S0    := ADS2*RDY286*WRT3*MIO3         ;286 S0,  HELD FOR 2 PHASE STAT CYCLE
       + ADS2*RDY286*CMD3*WRT3         ; 0 ALL OTHER TIMES
       + ADS2*RDY286*/MIO3*/CMD3*/WRT3
       + SFAZ1*S0
```

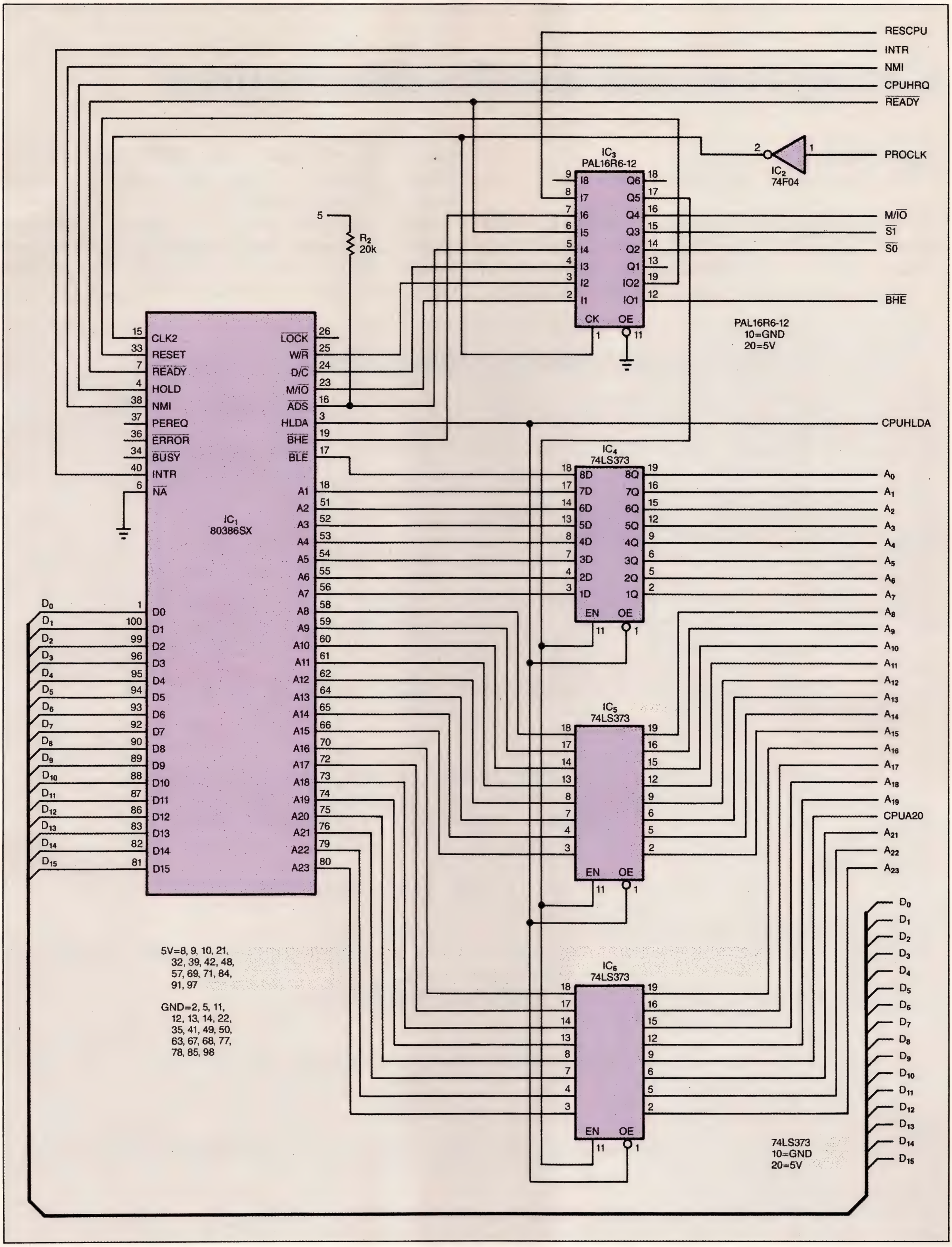


***Fig 1—With the aid of a PAL device and*** *a few latches, you can adapt the 386SX μP to IBM PC/AT chip sets.*

# C string comparer handles abbreviations

David Rankin
*Prime Computer, Framingham, MA*

The string-comparison routine in **Listing 1** is only slightly longer than the standard string-comparison routine "strcmp," but it identifies any abbreviation of a string as well as merely the string itself. The abbreviation need only have some of the letters of the full string in exactly the same order as they would occur in the full string to generate a "hit."

You could use this routine, for example, in an input-command processor for a program designed for both experienced and inexperienced users. Inexperienced users would enter the full name of the command; expe-

**LISTING 1—ABBREVIATION-HANDLING STRING COMPARER**

```
/* ==================================================== *
* strfit
* If the two words fit, return a zero.  Else return a
* non-zero.
* ==================================================== */
int strfit ( pattern, sample )
char *pattern, *sample;
{

/* See if the first letters match. */
if (toupper( *pattern ) != toupper( *sample ))
        return(-1);

/* See if every character in sample is found in pattern. */
while ( *sample != 0 )
        {

        /* Look for a character in pattern that matches
        * the current character in sample. */
        while (toupper( *pattern ) != toupper( *sample ))
                {

                /* Move to the next char in pattern. */
                pattern++;

                /* See if we have reached end of pattern */
                if ( *pattern == 0 )
                        return( -1 );
                }

        /* Move to the next char in sample. */
        sample++;
        }

/* We have successfully matched every char in sample to a
* char in pattern. */
return( 0 );

}
```

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SPECIFICATIONS

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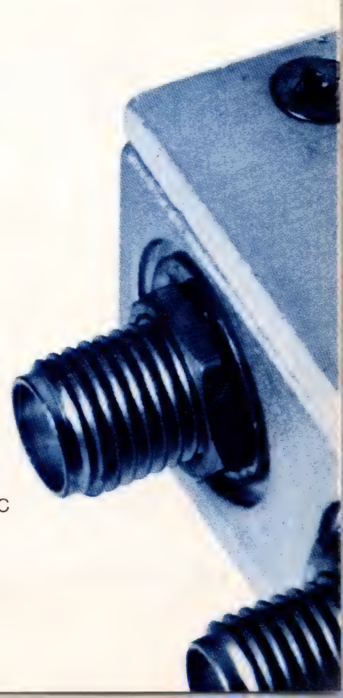
|---|---|---|---|---|
| Connector Version | **ZFSW-2-46** | | **ZFSWA-2-46** | |
| FREQ. RANGE | dc-4.6 GHz | | dc-4.6 GHz | |
| INSERT. LOSS (db) | typ | max | typ | max |
| dc-200MHz | 0.9 | 1.1 | 0.8 | 1.1 |
| 200-1000MHz | 1.0 | 1.3 | 0.9 | 1.3 |
| 1-4.6GHz | 1.3 | 1.7 | 1.5 | 2.6 |
| ISOLATION (dB) | typ | min | typ | min |
| dc-200MHz | 60 | 50 | 60 | 50 |
| 200-1000MHz | 45 | 40 | 50 | 40 |
| 1-4.6GHz | 30 | 23 | 30 | 25 |
| VSWR (typ) ON | 1.3:1 | | 1.3 | |
| OFF | — | | 1.4 | |
| SW. SPEED (nsec) rise or fall time | 2(typ) | | 3(typ) | |
| MAX RF INPUT (bBm) up to 500MHz | +17 | | +17 | |
| above 500MHz | +27 | | +27 | |
| CONTROL VOLT. | -8V on, OV off | | -8V on, OV off | |
| OPER/STOR TEMP. | -55° to +125°C | | -55° to +125°C | |
| **PRICE** (10-24) | **$32.95** **$69.95** | | **$48.95** **$79.95** | |



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CIRCLE NO 91

rienced users would be free to abbreviate the commands as they saw fit. Thus, you can concoct long, self-documenting names without saddling users with an onerous amount of typing; and users can democratically develop a set of abbreviations, within reasonable limits, that suits their fancies.

This routine, strfit, is a direct replacement for strcmp because its parameter list is the same. The first argument you must supply is the pattern word, such as the name of a command. The second argument is the user's input. Strfit's algorithm determines if all of the letters in the user's input appear in the pattern word in the same order. The algorithm ignores both intervening letters in the pattern word and the case of the letters. Additionally, the first letter in the user's input and the pattern word must match.

Thus, WordDump and wdmp generate a match, and DisassemblyMem and Dasm generate a match. WordDump and Dump don't generate a match because the first letters don't match; WordDump and WDpm don't generate a match because the letters are out of order.

Obviously, you must set up your list of commands so that all possible abbreviations match only one pattern word. As an error check, the routine that calls strfit could notify the user if it finds two matches for a given abbreviation. EDN

**To Vote For This Design, Circle No 749**

# 500-kHz switcher produces −5V

David Sherman
*Intermec, Lynnwood, WA*

The 500-kHz switching regulator in **Fig 1** produces −5V at 5 to 40 mA from a 5V supply. The circuit uses only surface-mount components. The output regulation is 4 mV for a load variation of 5 to 30 mA. The circuit's efficiency is 82% for a 37-mA load.

The **figure** shows $IC_{1A}$ and $IC_{1B}$ forming a standard 2-inverter oscillator. Obviously, you can substitute an appropriate system clock for this oscillator's output. The 500-kHz clock signal goes to a current-controlled, pulse-width modulator comprising $Q_1$, $D_1$, $C_2$, and Schmitt trigger $IC_{1C}$. This modulator generates a sawtooth waveform of variable slope across $C_2$, which results in a variable duty-cycle pulse train at the output of $IC_{1C}$. Pin 9 of $IC_{1C}$, shown connected to 5V, could also function as a power-down input. If you bring this

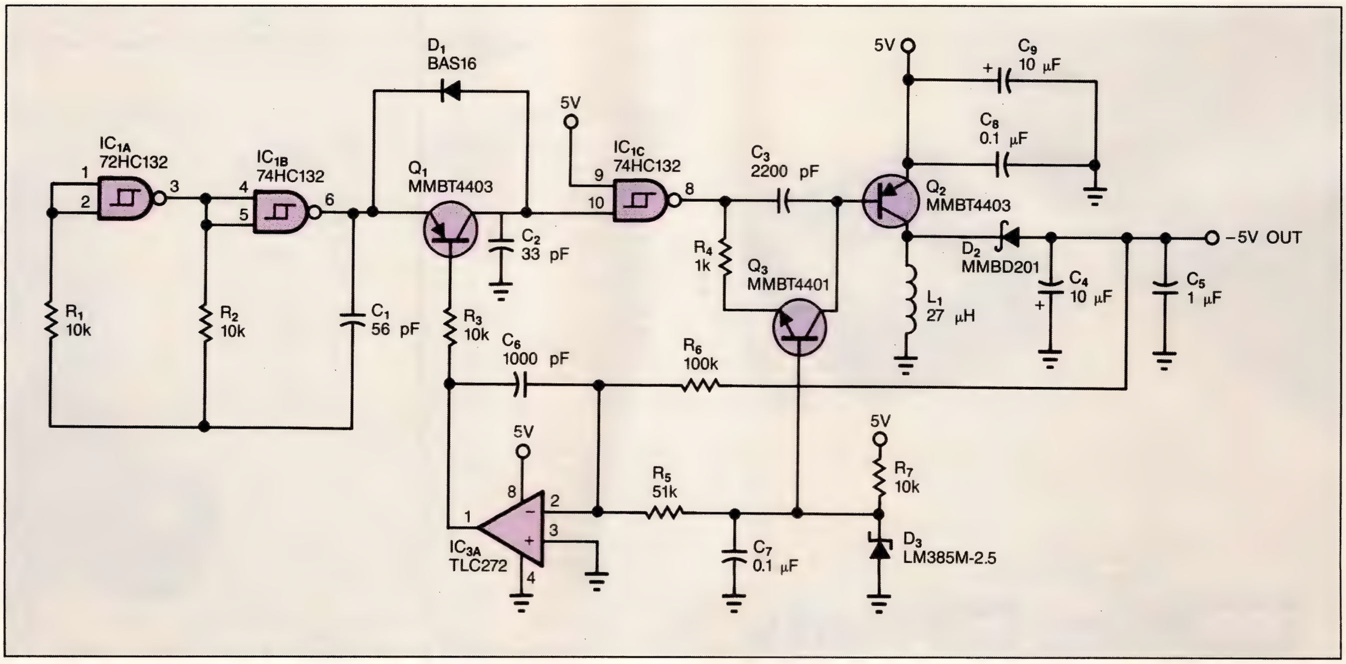


*Fig 1—**This 500-kHz switcher produces −5V from** a 5V supply and uses only surface-mount components.*


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pin low, the regulator will safely shut down in a low-power mode.

The key to this regulator's ability to switch a bipolar transistor efficiently at such a high frequency is the drive circuit, which comprises $C_3$, $R_4$, and $Q_3$. When the pulse-width modulator's output is low, a constant current of approximately 1.8 mA flows through $Q_2$'s base via $Q_3$. During this on-time, $C_3$ charges to 4.3V. Because of the excess charge stored in its base, $Q_2$ would ordinarily turn off slowly, but when the pulse-width modulator's output goes high, $C_3$ reverse biases the base of $Q_2$. $C_3$ then dispenses exactly enough charge to cancel out the stored charge in $Q_2$ and quickly stop current flowing through $Q_2$. Meanwhile, $Q_3$ also turns off rapidly because its biasing has prevented it from saturating. At this point, the voltage across $C_3$ is somewhat less than 3.2V because some of the charge has been removed.

When the pulse-width modulator's output once again goes low, a narrow, high-current pulse flows through the base of $Q_2$ to recharge $C_3$. This pulse also assures that $Q_2$ turns on rapidly. Then, $Q_3$ supplies the sustaining current described earlier.

This circuit uses a bipolar transistor for its switch instead of an FET because surface-mount FETs either require large amounts of pc-board area or have high on-resistances, which result in unacceptably low efficiencies. Furthermore, low on-resistance SOT-23 FETs are several times the price of SOT-23 bipolar transistors.

The remainder of this regulator is conventional. A small surface-mount inductor, $L_1$, such as TDK's NL453232-270K, provides energy storage; a Schottky diode, $D_2$, rectifies the output. $IC_{3A}$, which can be any single-supply op amp, serves as the error amplifier. If you need higher current, reduce the value of $L_1$; at lighter loads, increasing $L_1$ will boost efficiency. $R_5$ and $R_6$ set the ratio of output voltage to reference voltage. Thus, you can set the output level at any negative voltage within the breakdown limits of $D_2$ and $Q_2$. If your input-voltage level is sufficiently accurate and you do not need a reference for other circuitry, you can double $R_5$ and use the 5V input as the reference. In any case, the base of $Q_3$ must connect to a voltage between 2 and 3V that is bypassed with a 0.1-μF capacitor. EDN

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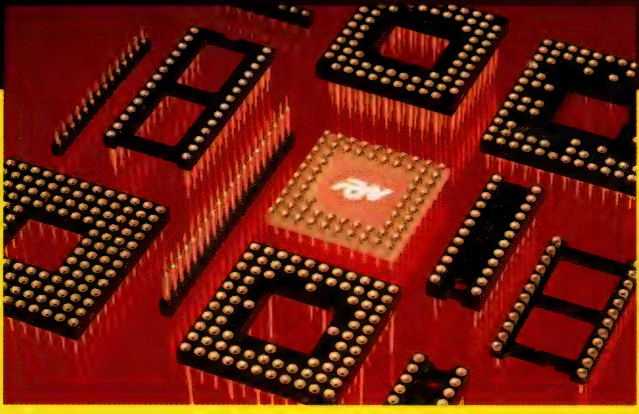

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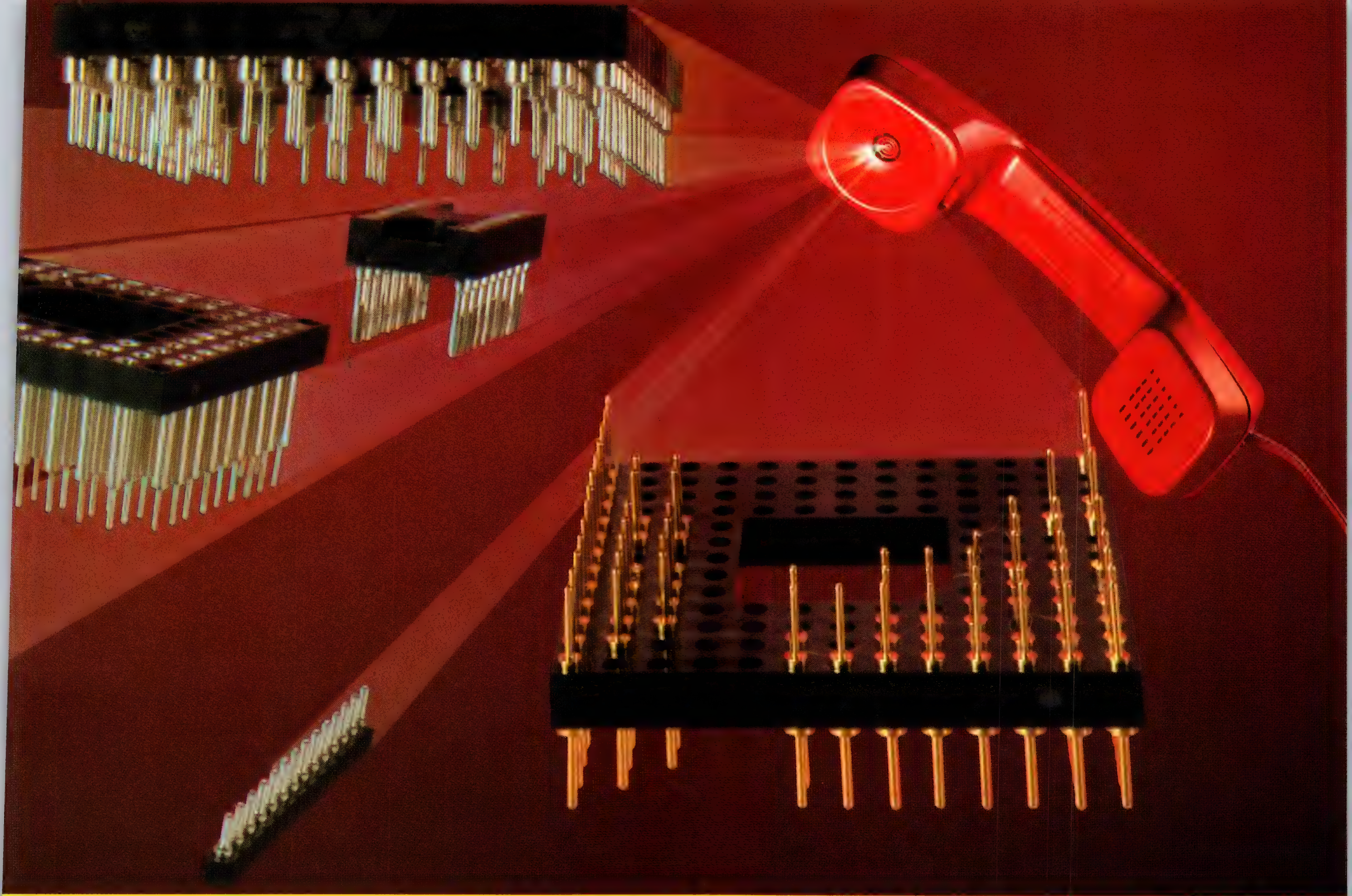

## COMPONENTS & POWER SUPPLIES

### DIGITAL PANEL METER

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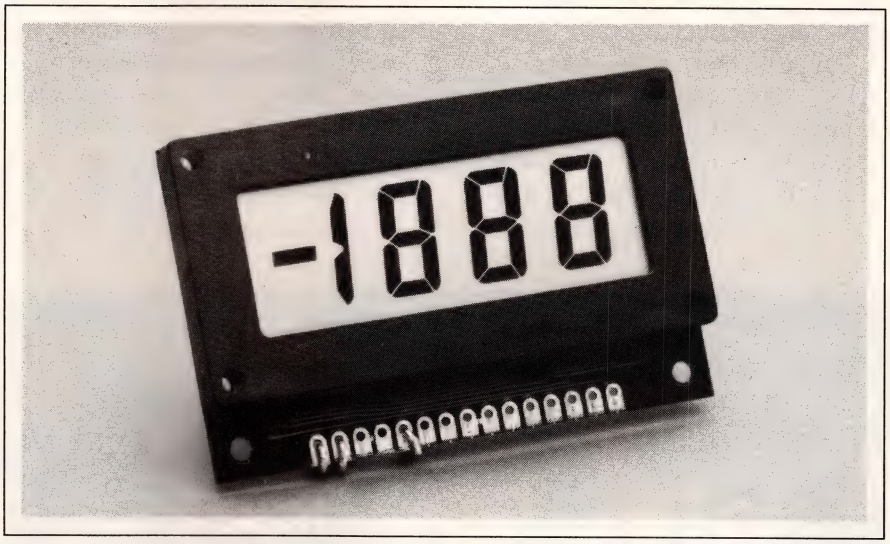


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**Circle No 351**


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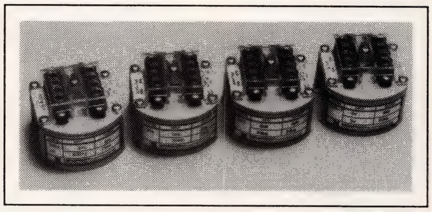

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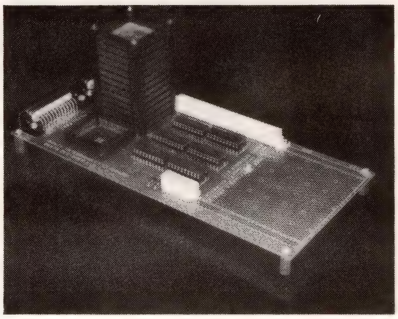
**Aromat Corp,** Industrial Products Div, 629 Central Ave, New Providence, NJ 07974. Phone (201) 464-3550. FAX 201-464-8513.

**Circle No 355**



## PROTOTYPING KIT

- *Allows you to evaluate a 3-dimensional interconnect system*
- *Provides a fully functional microcomputer*

The Chiprack Designer's Kit comprises a complete microcomputer system in a 7×4×4-cm component

stack and provides a practical example of the packing density attainable with the company's Chiprack 3-dimensional interconnection system. The stack contains a 68070 μP, an RS-232C interface, an ASIC that provides a memory interface and support logic for the μP, 64k bytes of one-time-programmable CMOS ROM for monitor software, and 64k bytes of CMOS static RAM. You can add other Chiprack carriers to increase the memory capacity to 512k bytes. The Chiprack stack is mounted on a mother board that contains a prototyping area and address- and data-bus buffers for the μP. Options include a PC-compatible interface card and a cross-assembler. Approximately £400 to £700.

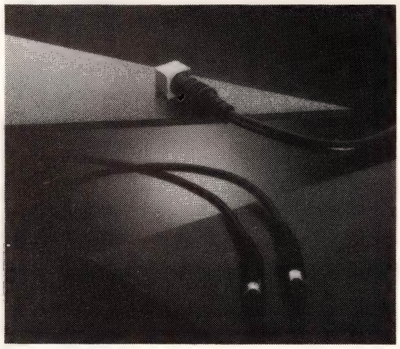
**Dowty Interconnect,** Knaves Beech Business Centre, Loudwater, High Wycombe, Buckinghamshire HP10 9UT, UK. Phone (0628) 810810. TLX 846874. FAX 0628-810813.

**Circle No 357**

**Dowty Interconnect,** 805 E 20th St, Santa Ana, CA 92706. Phone (714) 558-1295. FAX 714-752-6082.

**Circle No 358**





## CABLE ASSEMBLIES

- *Compatible with computer I/O interface*
- *Save pc-board space*

The Mini-Din connector provides pc-board space saving of 75% when compared with standard circular DIN connectors. It is available with three to eight contact positions, and Mini-Din plugs and sockets are compatible with the new generation IBM and Apple personal-computer I/O interfaces. Standard cable assemblies are available in 1, 2, and 3m lengths with beige or black overmold. The cable section incorporates 28 AWG stranded conductors with foil wrap/drain wire shielding and PVC jackets. The cables have a 500V ac voltage rating and a −40 to +70°C operating range. $5.19 (OEM qty) for a 1m plug/cable assembly.

**Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007. Phone (312) 981-6000.

**Circle No 356**

Text continued on pg 230

# "**EDN MAGAZINE'S** *PRODUCT MART SECTION IS HELPING US BECOME A LEADER IN OUR MARKETPLACE.*"

*Raymond J. Schnorr*
*Vice President of Marketing*
*ACCEL Technologies*

**As Vice President of Marketing, Ray Schnorr** is responsible for marketing ACCEL Technologies' affordable, professional software that meets the design needs of electrical engineers. He operates on a fixed budget and demands results. "When it comes to buying media, I'm interested in two things: performance and price. With EDN's Product Mart section, I pull high-volume sales leads and meet my budget," says Schnorr.

In nineteen months, ACCEL has sold 5000 software packages to 3000 sites. "Our 1/9-page Product Mart ads in EDN magazine are allowing us to reach our target audience." And Schnorr sees more for EDN and ACCEL. "We have significant growth plans for ACCEL, and running bigger ads in EDN will be part of the strategy to get there.

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ACCEL Technologies, 7358 Trade St., San Diego, CA 92121
Outside N., S. America contact HST Technology (Australia)
Phone: 61-02-34-8499 FAX: 61-02-25-8771

CIRCLE NO 347

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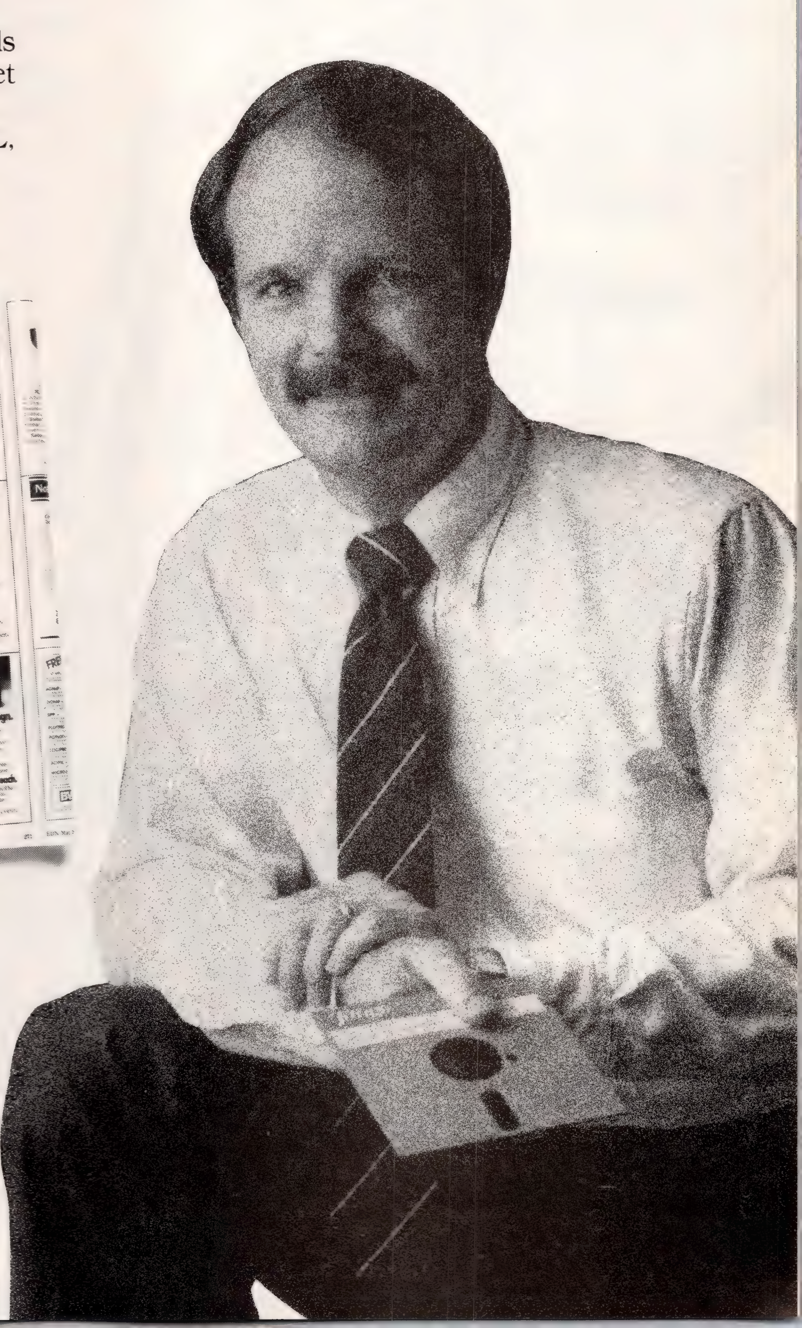
ACCEL Technologies, 7358 Trade St., San Diego, CA 92121

CIRCLE NO 348



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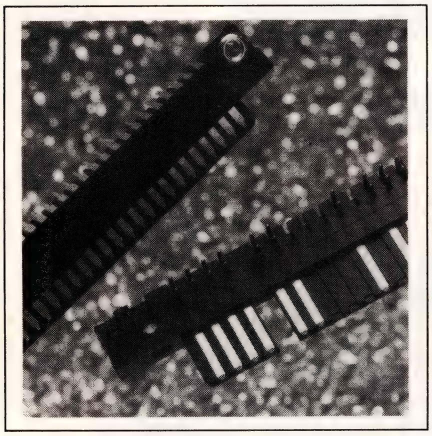


## CONNECTORS

- *Fully compatible with robotics*
- *Have 10 to 60 positions*

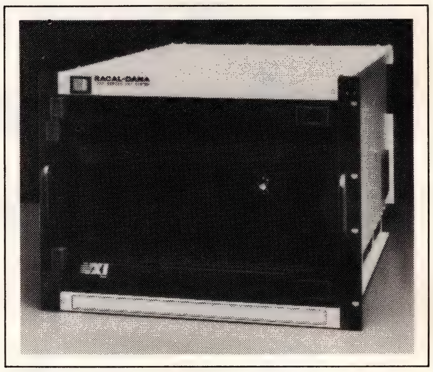
Edgemate connectors replace gold edges on daughter cards without requiring costly redesign. They feature recessed gold-plated fingers to prevent accidental peelback during mating. The connectors mate with any card-edge connector that has a 0.1-in. contact spacing. They are available with 10 to 60 positions and are fully compatible with robotics. Registration features and true-position solder legs aid in pick and placement operations. Top-activated eyelets eliminate the need for any ancillary tooling. The connectors come in tube packages to provide compatibility with automatic feed stations. $0.09 (1000). Delivery, six to 10 weeks ARO.

**AMP Inc,** Box 3608, Harrisburg, PA 17105. Phone (717) 564-0100. FAX 717-561-6179.

**Circle No 359**

## VXI BUS CHASSIS

- *Includes a power supply*
- *Designed for ATE applications*



This C-size VXI Bus chassis is designed for both military and commercial ATE applications. It features an 8-output power supply and a 12-layer backplane. DIP switches route the daisy-chained signals through the backplane, so you don't need jumpers to span empty slots in the chassis. A cable tray allows you to easily integrate VXI Bus instruments with other GPIB instrumentation. Rack cabling enters through recessed rear connectors and is cabled via the tray to the bus instruments. The tray also features a cover to minimize internal dust problems. A cooling system pulls air in through the sides of the

chassis and blows it out the rear. The chassis comes with a removable, hinged front door made of transparent plastic. $6350.

**Racal-Dana Instruments Inc,** 4 Goodyear St, Irvine, CA 92718. Phone (714) 859-8999. FAX 714-859-2505.

**Circle No 360**

## PRESSURE SENSORS

- *Have an extended operating range*
- *Feature a 100-mV output*

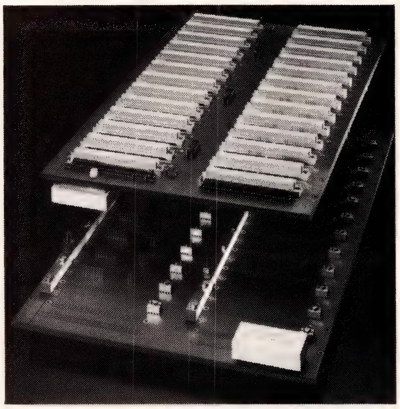
Pix Series pressure sensors use silicon-on-insulator (SOI) technology that extends the upper end of the operating range to 250°C. The sensors have a 0- to 100-psi range (0 to 700 kPa) and come in sealed-gauge versions. The devices have a 100-mV full-scale output (FSO) and operate from a 5-mA excitation. Nonlinearity of 0.1% FSO max and thermal errors of 3% FSO max are guaranteed over the full operating range. Stainless steel packages provide rugged housing for the chips. A thin, stainless-steel diaphragm isolates the chip from any harsh media, providing all-media compatibility. $250. Delivery, 10 weeks ARO for evaluation units.

**NovaSensor,** 1055 Mission Ct, Fremont, CA 94539. Phone (415) 490-9100.

**Circle No 361**

## BACKPLANE

- *Accommodates 13 VXI Bus modules*
- *Conforms to revision 1.2 of the VXI Bus specification*



This 13-slot VXI Bus backplane accepts A-, B-, or C-sized VXI Bus modules. It complies fully with revision 1.2 of the VXI Bus specification, and it has an active SUMbus protection module to monitor the bus voltage and accommodate the specified variations in load characteristics. The backplane uses an 8-layer board and strip-line construction to provide exceptionally low levels of crosstalk and immunity from interference or radiation. Approximately $1000.

**Bicc-Vero Electronics Ltd,** Electron Way, Chandlers Ford,

Eastleigh, Hants SO5 3ZR, UK. Phone (0703) 266300. FAX 0703-265126.

**Circle No 362**

**Bicc-Vero Electronics Inc,** 1000 Sherman Ave, Hamden, CT 06514. (203) 288-8001. FAX 203-287-0062.

**Circle No 363**

## OPTICAL LINK

- *Has a 2-km transmission distance capability*
- *Operates from 5V dc*

Operating at 1300 nm, the EDL-1300 Series fiber-optic data link transmits serial digital TTL data over multimode optical-fiber cable at distances in excess of 2 km. The link can accommodate data rates ranging to 50M bps. Each transmitter and receiver is housed in a 16-pin DIP, which contains an integral ST-compatible connector. The transmitter and receiver module operates over a 0-to-70°C range. The link loss-budget equals 15 dB. The module operates from a 5V dc supply and provides a direct interface with TTL circuitry. Transmitter/receiver set, $320.

**PCO Inc,** 20200 Sunburst St, Chatsworth, CA 91311. Phone (818) 700-1233.

**Circle No 364**

## CRYSTAL OSCILLATORS

- *Cover frequency range 375 kHz to 30 MHz*
- *Are housed in surface mounting packages*

QC6111 and QC6112 crystal oscillators are packaged in 40-pad, surface-mounting, ceramic leadless chip carriers. They cover frequencies from 375 kHz to 30 MHz. QC6111 devices drive two standard TTL loads or 50 pF at logic levels of 10 and 90% of their supply voltage, and their maximum power dissipation ranges from 55 to 90 mW. QC6112 devices drive 10 standard TTL loads at TTL-compatible logic levels, and have power dissipations from 130 to 250 mW. Both series achieve maximum rise and fall times of 10 nsec. Versions with operating temperature ranges of −40 to +85°C are available with stabilities over ±35 or ±60 ppm. Versions with operating temperature ranges of −55 to +125°C are available with stabilities over ±60 or ±100 ppm. All of the oscillators operate from a 5V ±10% supply. £40 to £50 for sample quantities.

**Salford Electrical Instruments Ltd** Times Mill, Heywood, Lancashire OL10 4NE, UK. Phone (0706) 67501. TLX 635106. FAX 0706-64394.

**Circle No 365**

CIRCLE NO 120

# "SWITCH DC TO HUNDREDS OF MHz IN 8x8 to 64x8 CONFIGURATIONS"

It's easy to switch eight DC to 500Mhz inputs to any of eight outputs with our Model 4108 wide-band coaxial relay matrix shown at the left. This miniaturized matrix is completely self-contained, requiring only TTL control signals and DC power.

For larger systems, our Model 4076 can switch 64 signal sources to any of eight outputs under IEEE-488 control with a bandwidth of DC-300Mhz by packaging up to eight 4108 modules in a compact cabinet.

These miniaturized extremely wide-band matrices are perfect for Automatic Test Equipment (ATE) where fast rise time, wide bandwidth data from the unit under test must be connected to any array of test equipment, or in telecommunications where wideband data rates must be connected between modems, transceivers or satellite uplink/downlink terminals.

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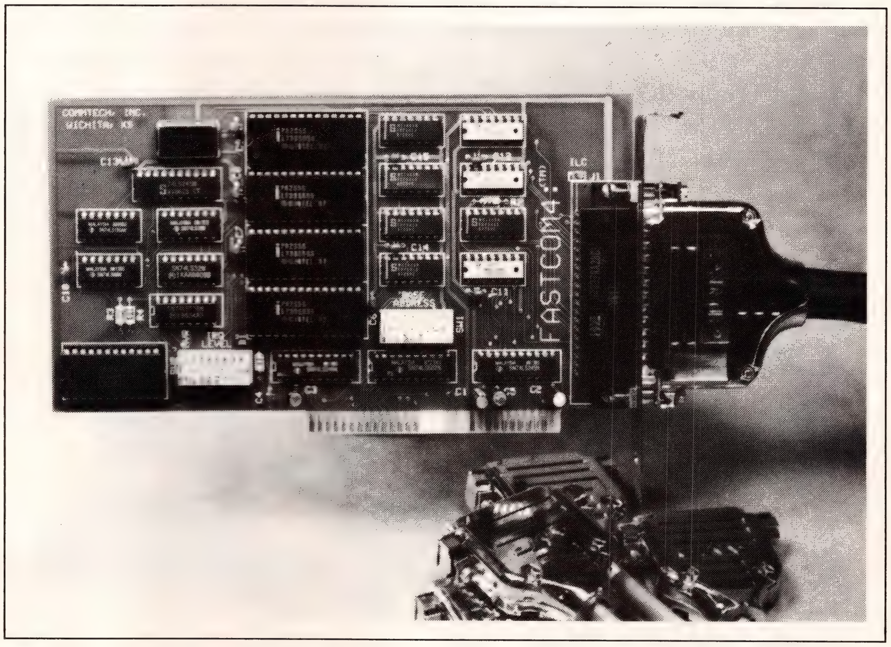
CIRCLE NO 121

## RS-232C ADAPTER

- *Provides four serial ports for the IBM PC, PC/XT, and PC/AT*
- *Uses the Intel 82050 or the 82510 UART*




The FASTCOM4 is a 4-channel RS-232C board for the IBM PC, PC/XT, PC/AT, and compatible computers. The standard configuration uses Intel's 82050 UART, which is fully compatible with the 16450 UART but draws only one-half the power. The board is optionally available with Intel's 82510 UART. The 82510 offers baud rates as high as 288k bps, a 4-byte receive and transmit buffer, control character recognition, and two independent baud-rate generators. The board comes with COMMBIOS and COMMBUFF software development tools. COMMBIOS has interfaces for Pascal, Turbo Pascal, Lattice C, Microsoft C, Compiled Basic, and Fortran. COMMBUFF is a high-speed buffer program which allocates 4k bytes of buffer memory per channel. The board has a shared interrupt feature that allows as many as four boards (16 channels) to be installed in a computer. $375. Optional 82510 UARTs, $25 each. An optional NVRAM that stores 32 bytes of nonvolatile data, $35.

**Commtech Inc,** 8622 Mt Vernon Ct, Wichita, KS 67207. Phone (316) 651-0077.

**Circle No 370**

## SPARC COPROCESSOR

- *Board for the IBM PC/AT computer runs on MS-DOS*
- *Uses Cypress CY7C601 SPARC chip*

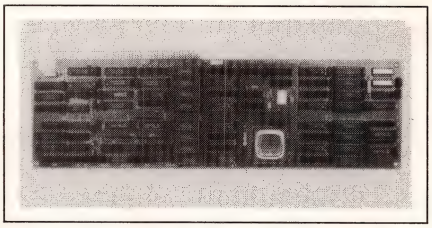
The SP-ARC1 is a coprocessor board for the IBM PC/AT and compatible computers. It features the Cypress CY7C601 SPARC Chip, TI's TI8847 floating-point processor, and as much as 8M bytes of interleaved DRAM—all running at 20 MHz to deliver 12 MIPS performance. The board comes with C and FORTRAN compilers, which are derived from SUN's compilers for the Sun-4 workstation. The board lets you run software developed for the Sun-4 workstation in MS-DOS applications. Essentially, the board becomes the system CPU while the host's CPU acts as an I/O processor. The board uses the host CPU to access peripherals such as graphics cards, A/D converters, disk controllers, and communication boards. A 4M-byte system, including compilers, costs $7995. The same system with 8M bytes costs $9995.

**Definicon Systems Inc,** 1100 Business Center Circle, Newbury Park, CA 91320. Phone (805) 499-0652. FAX 805-498-3559. TLX 272849.

**Circle No 371**

## ARRAY PROCESSOR

- *Accelerates image processing for the IBM PC/AT computer*
- *32-bit floating-point processor that delivers 13.3M flops*



The ASAP32 is an array-processor board for the IBM PC/AT and compatible computers. The board accelerates image processing using a 32-bit floating-point processor that delivers 13.3M flops. The board contains 2k × 32-bits of ROM and RAM space for storing programs. The ROM contains all of the basic mathematical, vector, and I/O functions. The host loads the RAM with microcode to execute the desired function. In addition, it contains two 4k × 32-bit static RAMs for transferring data between the frame buffer and the floating-point processor. Both SRAMs have dual ports permitting pipeline operation, alleviating bottlenecks on the PC bus. The board has an extensive set of software libraries, including image filtering, image geometry, and

a 2-dimensional FFT. The libraries are software compatible with Image Technology's ITEX call conventions. $1350. Delivery, four to six weeks ARO.

**Rapid Technology Corp,** 54 Ballard St, Newton, MA 02159. Phone (617) 244-7928. FAX 617-527-3177.

**Circle No 372**

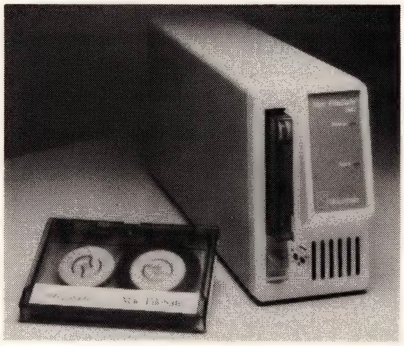
## COLOR PRINTER

- *Prints Adobe Postscript images at 300 dpi*
- *Uses thermal transfer for A or B size paper and transparencies*

The 5232-Color Postscript Printer prints Adobe Postscript images and text at 300 dpi on A or B size paper and transparencies. There are three ink sheets available: 4-color (yellow, magenta, cyan, black); 3-color (yellow, magenta, cyan); and monochrome (black). The print controller uses a 16-MHz 68020 µP and either 4M bytes of RAM for A size printing or 8M bytes for B size printing. It has 35 Adobe resident fonts in ROM and supports downloadable fonts. The printer interfaces with a host through an RS-232C/422/423 serial port or a Centronics parallel port. It can print a 3-color A size drawing in 90 sec; a B size drawing takes 180 sec. An internal 20M- or 80M- byte disk drive is also available. Prices range from $16,900 to $22,900.

**Schlumberger Graphics,** 385 Ravendale Dr, Box 7169, Mountain View, CA 94039. Phone (415) 964-7900. FAX 415-961-6152. TLX 491178.

**Circle No 373**



## TAPE BACKUP

- *System for the Macintosh computers stores 150M bytes*
- *Performs image backup on a MAC II at 6M bytes/min*

The MAC Filesafe 150 is a streaming tape backup system for the Macintosh SE and Macintosh II

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New Brighton, MN 55112

**CIRCLE NO 78**

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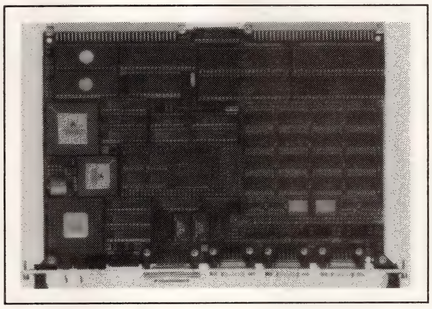
computers. It stores 150M bytes of formatted data on an industry standard DC600XTD quarter-inch cartridge using the QIC-150 format. The stand-alone system comes in a half-height, 5¼-in. form factor and uses a SCSI interface to communicate with the host. The unit can perform an image backup on the Macintosh II computer at 6M bytes/min for a total back-up time of 25 min. The unit verifies all written data and automatically skips any bad blocks. Its software features include one-step automatic installation, menu guidance, on-line help, automatic back-up, separate tape verification, restore, tape directory, and user settable defaults. $2195.00

**Mountain Computer Inc,** 240 Hacienda Ave, Campbell, CA 95008. Phone (408) 379-4300. FAX 408-379-4302.

**Circle No 374**



## CPU CARD

- *Runs a 68020 μP at clock speeds as high as 25 MHz*
- *Includes parallel, serial, SCSI and Ethernet interfaces*

Provided with 38 fully programmable bidirectional parallel I/O lines, the SYS68K/CPU-27 CPU card for VME bus systems is suited for use in industrial control applications. The board runs a 12.5-, 16.7-, or 25-MHz 68020 μP and a 68882 math coprocessor. It has 1M bytes of onboard static RAM, and two JEDEC compatible EPROM sockets that can accommodate 8M-bit devices when the devices become available. The board is supplied with these sockets occupied by the company's VMEPROM real-time kernel. The board has an additional 32k bytes of static RAM with onboard battery backup. Its parallel I/O lines are controlled by two 68230 parallel interface/timer chips, and the board has three serial I/O ports, two of which are configurable for RS-232C, -422, or -485 operation, while the third supports RS-232C only. The board also has a SCSI bus interface, and an optional Ethernet interface with its own 64k-byte buffer. Software development support is available for use under the PDOS operating system. Alternatively, you can use VMEPROM's link software to link the board to Unix 5.3 or MS-DOS operating systems. From around DM 7800 to DM 11,000.

**Force Computers GmbH,** Daimlerstrasse 9, 8012 Ottobrunn/Munich, West Germany. Phone (089) 600910. TLX 524190. FAX 089-6097793.

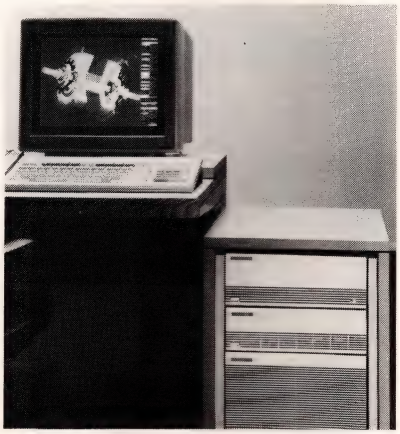
**Circle No 375**

**Force Computers Inc,** 3165 Winchester Blvd, Campbell, CA 95008. Phone (408) 354-3410. TLX 172465. FAX 408-395-7718.

**Circle No 376**

## 3D WORKSTATION

- *Contains a 68030 µP and 68882 coprocessor delivering 4 MIPS*
- *Is source- and object-code compatible with the 9000 series 300*



The HP 9000 Model 340SRX 3D graphics workstation contains a 68030 µP and a 68882 coprocessor, which deliver a 4-MIPS performance rating. The model is source- and object-code compatible with the company's 9000 series 300 computers. In addition, it contains 4M bytes of RAM expandable to 16M bytes, a 16-in. color monitor with 1280×1024-pixel resolution, and the company's SRX graphics subsystem, which can be expanded from 8 to 32 color planes. The system is compatible with a range of 3D mechanical CAE and CAD software available from McDonnell Douglas, PDA Engineering, and Swanson Analysis. The system runs on the company's HP-UX operating system, which adhers to AT&T's UNIX System V Interface Definition Issue 2. $14,900.

**Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

**Circle No 377**

## SECURITY DEVICE

- *Prevents unauthorized access to modems*
- *Device requires a caller to have a password and a phone number*

The 232MSD Modem Security Device protects computers or private bulletin boards against unauthorized access. It works with most stand-alone modems that are compatible with the Hayes AT command set. The device uses a call-back method for protection. When

a caller reaches the modem, the device intercepts the call and asks for a password. After validating the password, it requests the caller to hang up. The device then calls a phone number, stored in memory, associated with the password. The user at that phone number is then allowed access to the computer. If a hacker steals a user's password, the password is unusable because the thief will not be at the user's phone number. The unit features a 50-number directory of password/phone number combinations, EEPROM storage for power-failure protection, and a systems manager that can disable the call-back procedure as an alternative. $129.95.


**B&B Electronics,** 4000 Baker Rd, Box 1040, Ottawa, IL 61350. Phone (815) 434-0846. FAX 815-434-7094.

**Circle No 378**

## DISPLAY CARD

- *Drives 1280×960 pixels for the Macintosh II computer*
- *Provides 256 colors from a pallette of 16.7 million colors.*

The nuVista HR is a plug-in display card for the Macintosh II computer that can drive a display with 1280×960 pixel resolution. It can simultaneously display 256 colors from a pallete of 16.7 million colors. A 2M-byte version of the card provides a virtual canvas of 2k×1k pixels, and a 4M-byte version provides a virtual canvas of 2k×2k pixels. The card uses the TI 34010 graphics processor for graphics manipulations. It also drives non-interlaced displays, provides square pixels, and can pan the entire video memory. It works with high resolution monitors with 64 kHz horizontal and 60 Hz vertical frequencies, such as Sony's GDM-1953 or JVC's GD-H6020US. The board is fully compatible with Apple's QuickDraw software package. The card can accommodate an additional 2M, 4M, or 8M bytes of memory using an optional NuVMX memory expansion module. 2M-byte version, $3995; 4M-byte version, $5995.

**Truevision Inc,** 7351 Shadeland Station, Indianapolis, IN 46256. Phone (800) 858-8783 or (317) 841-0332. FAX 317-576-7700.

**Circle No 379**

# "I'M A TRUE BELIEVER IN THE POWER OF **EDN MAGAZINE**."

*Robert E. Sanders*
*Manager, Marketing Communications*
*Rogers Corporation*

**Bob Sanders is a pro at marketing materials and** components for Rogers Corporation, a worldwide leader with divisions from Connecticut to Arizona. To do the best job, he uses EDN magazine.

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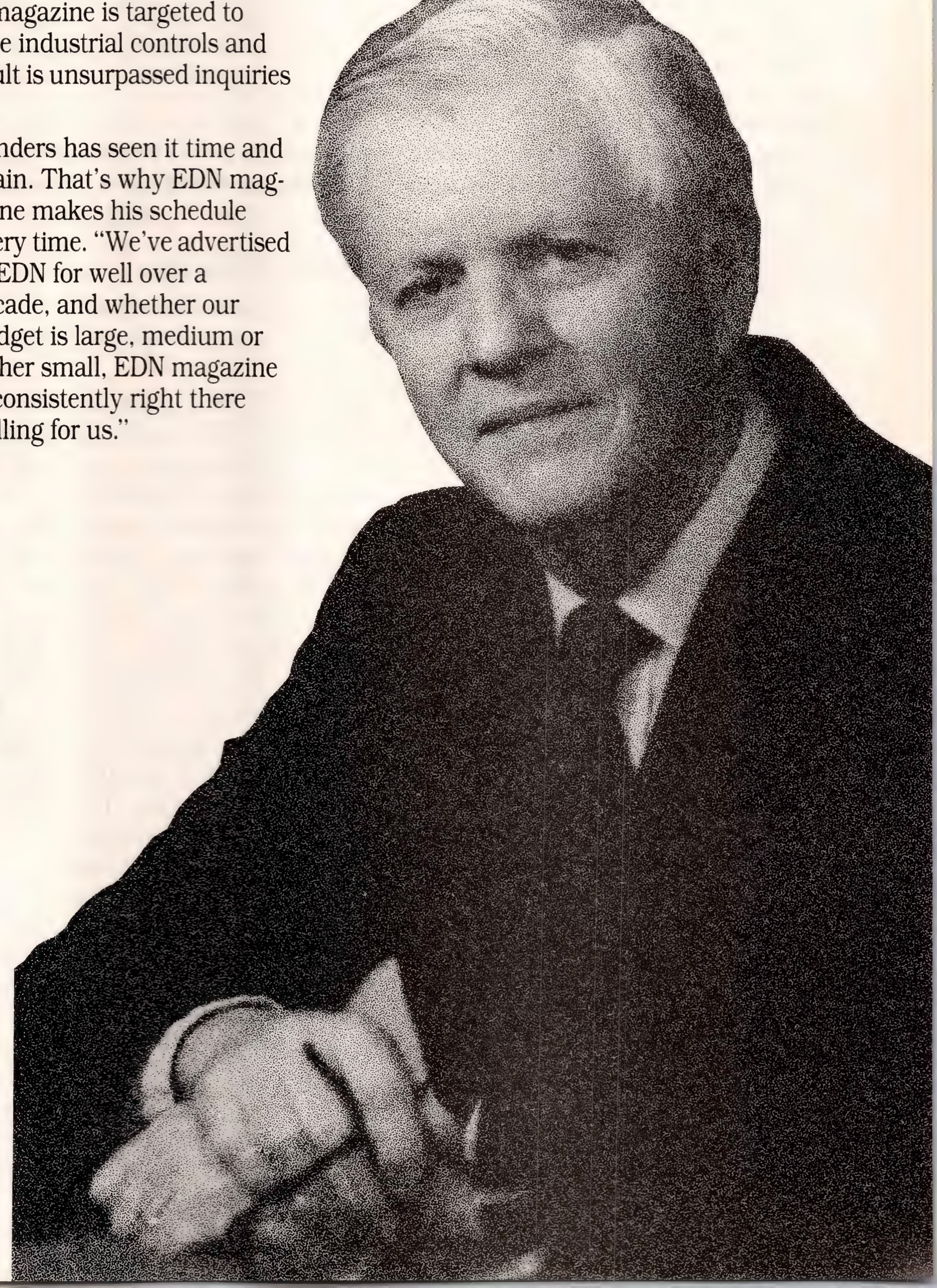
Sanders has seen it time and again. That's why EDN magazine makes his schedule every time. "We've advertised in EDN for well over a decade, and whether our budget is large, medium or rather small, EDN magazine is consistently right there pulling for us."



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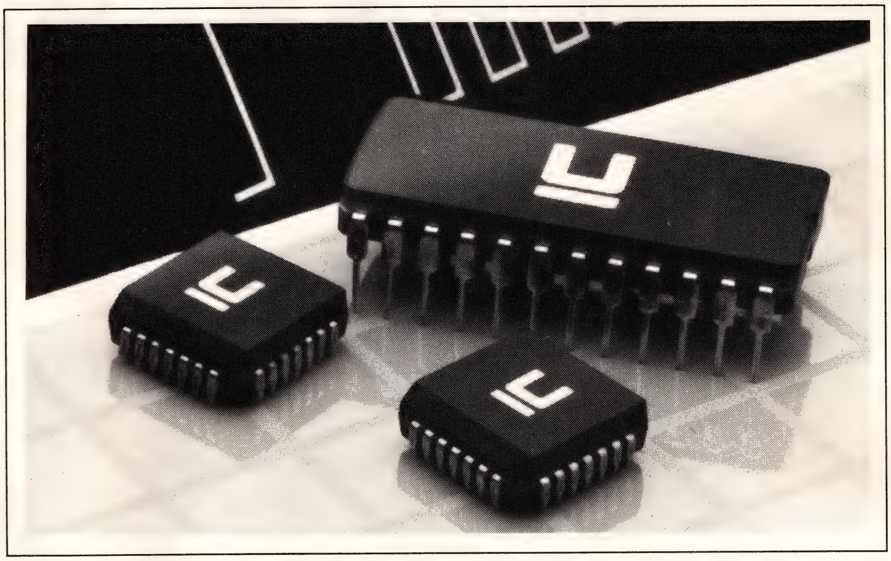
## INTEGRATED CIRCUITS

### MOTOR CONTROLLER

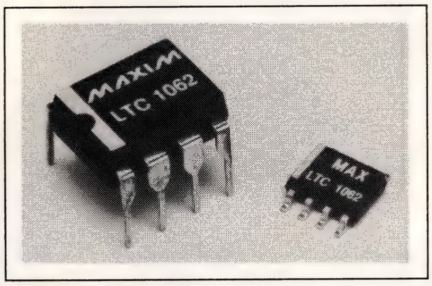
- *For three-phase brushless motors*
- *Contains Hall-cell decode logic*

Combining in one IC all the functions required of a three-phase brushless motor controller, the UC3625 has separate outputs to control six power switches. The IC features Hall-cell decode logic with built-in cross-conduction protection. Other features include a tachometer, soft start, under- and over-voltage protection, current-controlled braking, and selection of either two- or four-quadrant operation. The UC3625 includes hysteretic comparators on all logic inputs and noise blanking at the Hall-cell inputs. The IC also includes a direction latch, absolute-value current sensing, and a precision reference voltage. 28-pin DIP, $5.85 (100).



**Unitrode Integrated Circuits,** 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410.

**Circle No 385**




### LOWPASS FILTER

- *Fifth-order Butterworth type*
- *DC to 20 kHz cutoff frequency*

The LTC1062 switched-capacitor filter is clock tunable from dc to 20 kHz with an external resistor and capacitor and features a cutoff frequency accurate to 1%. The LTC1062 functions as a fifth-order lowpass filter, and you can cascade two devices to form a tenth-order filter. The device, which also features a buffered output, is available in commercial and military temperature ranges in 8-pin DIP and 16-pin SO packages. Prices start at $3.30 (100).

**Maxim Integrated Products,** 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

**Circle No 386**

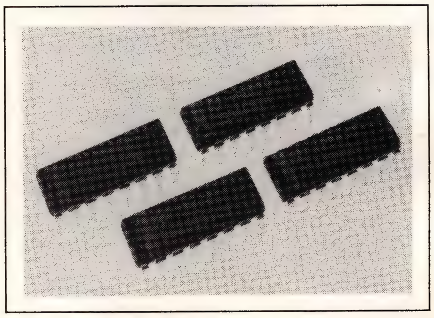
### CMOS EPROMs

- *Organized as 8k × 8 bits*
- *Three speed versions are available*

The 27HC64 high-speed 64k-bit CMOS EPROM has a JEDEC-standard EPROM pinout. The 27HC641 offers a bipolar PROM pinout. Both parts are available in 45-, 55-, and 70-nsec versions. Because of the CMOS process, the chips consume less power than do their bipolar counterparts. Also, unlike bipolar PROMs, the 27HC64 and 27HC641 are completely tested and then erased before shipment, thus ensuring the highest possible yield on customer patterns. The 27HC64 and 27HC641 are available in standard window ceramic DIPs, plastic DIPs, and surface-mount PLCC and LCC packages. The 27HC641 is also available in a window skinny ceramic DIP and a skinny plastic DIP. From $12.70 (1000).

**Microchip Technology Inc,** 2355 W Chandler Blvd, Chandler, AZ 85224. Phone (602) 963-7373. FAX 602-899-9210. TWX 910-950-1963.

**Circle No 387**



### DRIVERS/RECEIVERS

- *RS-422 compatible*
- *Fabricated in CMOS*

Matching the speeds of bipolar devices but consuming less power, the CMOS DS34C87/DS26C31 and DS34C86/DS26C32 are quad-differential line drivers and receivers, respectively. The drivers accept TTL or CMOS input levels and translate them to RS-422 output levels. Special output circuitry enables the individual drivers to power down without loading down the bus. The DS34C87 driver has separate enable circuitry for each pair of drivers; the DS26C31 has enable and disable circuitry that is common to all four drivers. Propagation delay is 11 nsec max. The receivers have

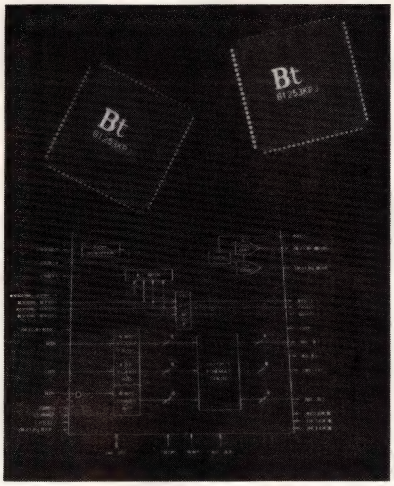
an input sensitivity of 200 mV over the common-mode input range of ±7V. Input hysteresis is typically 60 mV and propagation delay is 27 nsec max. The DS34C86 has separate enable pins; the DS26C32 has a common enable and disable function. Prices start at $2.85 (100).

**National Semiconductor Corp,** Box 58090, Santa Clara, CA 95052. Phone (408) 721-4474. TLX 346353.

**Circle No 388**

## IMAGE DIGITIZERS

- *Digitize at 15 MSPS rate*
- *Monochrome and color versions*




The Bt251 and Bt253 image digitizers provide the circuit designer with a means to add image-capture capability to PCs and workstations. The Bt251, which generates 8 bits of intensity information for each pixel, is a 15-MSPS single-channel device for digitizing monochrome (gray-scale) video signals. It supports four analog video inputs and contains an 8-bit A/D converter and a 256×8-bit lookup-table RAM. The Bt253 is a 15-MSPS device for digitizing three channels of color analog video signals (such as RGB) or a monochrome signal, using only the green channel. The Bt253, which generates 8, 15, or 24 bits of color information for each pixel, contains three 8-bit A/D converters and supports two separate three-channel video input ports. Bt251 (44-pin PLCC), $36; Bt253 (84-pin PLCC), $48 (100).

**Brooktree Corp,** 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 535-3251. TLX 383596.

**Circle No 389**

## HV DISPLAY DRIVERS

- *Provide 50 to 100V p-p output*
- *Have rise times from 2.5 to 4.5 nsec*

The 1902 high-voltage CRT drivers feature output drive capabilities from 50 to 100V p-p into a 10-pF load (the typical capacitance of a high-resolution CRT). Corresponding maximum rise and fall times range from 2.5 to 4.5 nsec. The devices are RS-170 and RS-343 com-

patible, and can be driven directly from a standard video DAC. Additional features include a 25,000V/μsec slew rate and a 40-dB CMRR. The line has five basic variants that define the output voltage and rise/fall times, and the devices come in hermetic, 30-pin flat paks with mounting flanges. Commercial parts, $185; MIL-STD-883 parts, $255 (100).

**Teledyne Philbrick,** 40 Allied Dr, Dedham, MA 02026. Phone (617) 329-1600.

**Circle No 390**

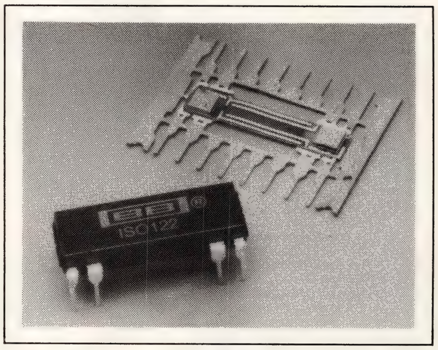
## COLOR RAM-DAC

- *Includes 256×18-bit RAM*
- *Includes three 6-bit DACs*

The ADV476 monolithic IC contains a 256×18-bit color-palette RAM, three 6-bit DACs, a latch circuit, a pixel read-mask register, bus control, an address register, and video RGB outputs. The RAM-DAC provides complete pixel management and output drive for VGA color-graphics displays. Using its 256×18-bit color look-up table, the ADV476 can simultaneously display 256 colors from a palette of 262,144 addressable colors. By writing to the pixel mask register, the system CPU can access different sections of the color look-up table and alter the displayed colors. The video RGB outputs are RS-170 and RS-343 compatible with no need for external buffering. The CMOS device comes in a 28-pin plastic DIP, operates from a 5V supply, and dissipates a maximum of 800 mW. The ADV476 is available in clock rates of 35, 50, and 66 MHz. $16, $17, and $20 (100).

**Analog Devices,** 804 Woburn St, Wilmington, MA 01887. Phone (617) 935-5565.

**Circle No 391**




## ISOLATION AMP

- *Provides 1500V isolation*
- *Operates from ±4.5 to ±18V supply*

Packaged in a compact 16-pin DIP, the ISO122P unity-gain amplifier has a minimum isolation-voltage rating of 1500 Vrms and a breakdown-voltage rating of 2400 Vrms. Isolation-mode rejection (IMR) is typically 140 dB at 60 Hz. Barrier leakage is only 0.5 μA max at 240V, 60 Hz. The ISO122P has an input/output voltage range of ±10V. The

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small-signal bandwidth is 50 kHz, and the gain error is typically 1±0.05% FSR. The two-chip hybrid IC's supply range of ±4.5 to ±18V lets designers use the part in standard bipolar (15V) and PC-based data acquisition systems. $9.50 (100).

**Burr-Brown Corp,** Box 11400, Tucson, AZ 85734. Phone (800) 548-6132.

**Circle No 392**

## COMPARATOR

- *Provides eight high-speed latched comparators*
- *Is suitable for 5 to 10V single- or split-supply operation*

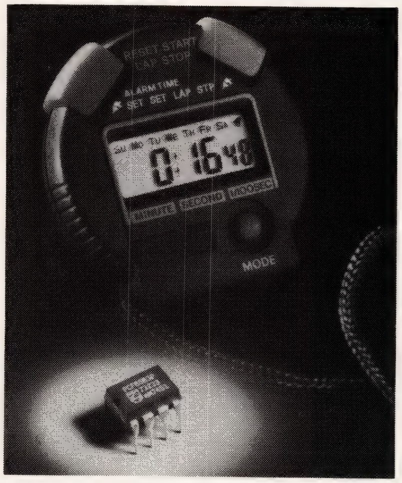
The SCC8008 octal comparator contains eight high-speed comparators with latched outputs. The comparators are divided into two groups of four; each group has its own buffered clock input. The two groups also have independent power supplies and bandgap-reference bias generators, allowing you to operate them from different supply voltages—such as in mixed TTL and ECL logic systems. You can achieve a variety of level-shifting functions by connecting the outputs of one group to the inputs of the other. In transparent mode, the comparators have a differential gain of 26 dB and a typical propagation delay for 10-mV input overdrive of 1.1 nsec. In the latching mode, the delay between the clock input and valid latched data is typically 0.8 nsec for 10-mV overdrive, and the output-to-output skew is 0.1 nsec max. The comparator's common-mode input-voltage range is 2.7V to ($V_{CC}-0.7V$), and the inputs have a typical input impedance of 300 kΩ. The SCC8008 is packaged in a 68-pad leadless chip carrier and has an operating temperature range of −40 to +85°C. Approximately £20 (100).

**STC Components,** Semiconductor Division, Maidstone Rd, Sidcup, Kent DA14 5HT, UK. Phone 01-300-3333. TLX 21836. FAX 01-300-9609.

**Circle No 393**

**STC Components Inc,** 636 Remington Rd, Schaumburg, IL 60173. Phone (312) 490-7150. FAX 312-490-9707.

**Circle No 394**



## CLOCK/TIMER/RAM

- *Includes clock/calendar, timer/counter, and RAM functions*
- *Remains operational on a supply voltage as low as 1V*

The PCF8583 incorporates a 256-byte static RAM and a real-time clock/calendar, which you can reconfigure to operate as an event counter. It is available in an 8-pin DIP, small-outline surface-mounting package, or as a naked die part. The device operates from a 2.5 to 6V supply and typically draws 10 μA of supply current. In standby mode it typically draws 2 μA, and its static RAM and clock/timer remain active at supply voltages as low as 1V. The device's real-time clock calendar operates in a 12- or 24-hour mode, and provides year (with leap-year compensation), month, day, day of week, hour, minute, second, tenths of a second, and hundredths of a second information. You can also program it to provide an alarm on specified dates, days, and times via a status bit or interrupt. The clock/calendar oper-

ates with a 32.768-kHz crystal, or a 50-Hz external clock input. In the event-counting mode the device can count as many as one million events applied to one of its oscillator input pins. You can also generate alarms on specified count values and on counter overflow conditions. The device's control/status register and clock/calendar information occupy the first 16 bytes of the RAM. All registers and memory locations in the PCF8583 are accessed via the device's $I^2C$ bus interface. Around $3 (50k).

**Philips,** Components Division, Box 218, 5600 MD Eindhoven, Netherlands. Phone (040) 757189. TLX 51573.

**Circle No 395**

**Signetics Corp,** 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

**Circle No 396**

## DECODER/DRIVER

- *Has 25 mA drive capability*
- *Quiescent current is 100 µA max*

The MIC4350, which draws a quiescent current of less than 100 µA, provides as much as 25 mA of drive per display segment, eliminating the need for additional drivers. The MIC4350 contains a counter, a 4-bit latch, and a seven-segment decoder/driver. The IC will drive displays that require current sinking in the active mode. Other features include synchronous or asynchronous operation, lamp blanking for intensity modulation, and leading-zero suppression. The CMOS MIC4350 is a pin-compatible replacement for the bipolar Motorola MC4050L/P. 16-pin DIP, $14.65 (100).

**Micrel Semiconductor,** 560 Oakmead Pkwy, Sunnyvale, CA 94086. Phone (408) 245-2500. FAX 408-245-4175.

**Circle No 397**

## CAE & SOFTWARE DEVELOPMENT TOOLS

### LOGIC SYNTHESIZER

- *Lets you correct logic errors without leaving the simulator*
- *Provides input-slew-rate modeling for macrocells*

The Ikos Simulation System Release 3.0 incorporates several new features. The Incremental Logic Synthesis (ILS) feature allows you to modify a circuit without leaving the simulator and automatically recompile changed portions of the net list. The ILS feature also allows you to initialize a node to a known value before simulation and force a node to a specified signal value during simulation. Other features include input-slew-rate modeling, which adds a slew-rate-dependent delay to the input of every macrocell model; back-annotation of RC wiring delays derived from actual layouts; a vector-grading feature that lets you analyze the effectiveness of test-vector sets; and spike and violation logging for generating a complete report on the activity. Complete simulation system including ILS, $64,000.

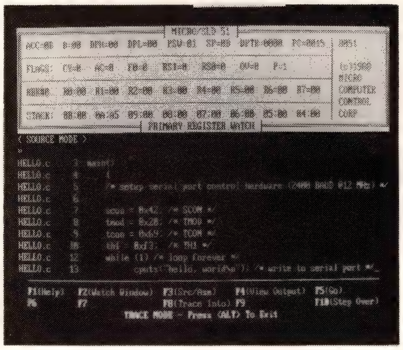
**Ikos Systems Inc,** 145 N Wolfe Rd, Sunnyvale, CA 94086. Phone (408) 245-1900. FAX 408-245-6219.

**Circle No 400**

### 8051 DEBUGGER

- *Provides C and assembler debugging facilities*
- *Executes 8051 or 8052 code on an IBM PC or compatible*

The MICRO/SLD-51 symbolic debugger executes 8051 or 8052 machine code on an IBM PC or compatible development host. The built-in



8051 simulator means that you don't need any additional hardware such as the target system or an in-circuit emulator to debug your programs. You can step through a C or assembly-language program, line by line, displaying the C or assembly-language source code as well as the contents of 8051 hardware registers and data variables stored in mem-

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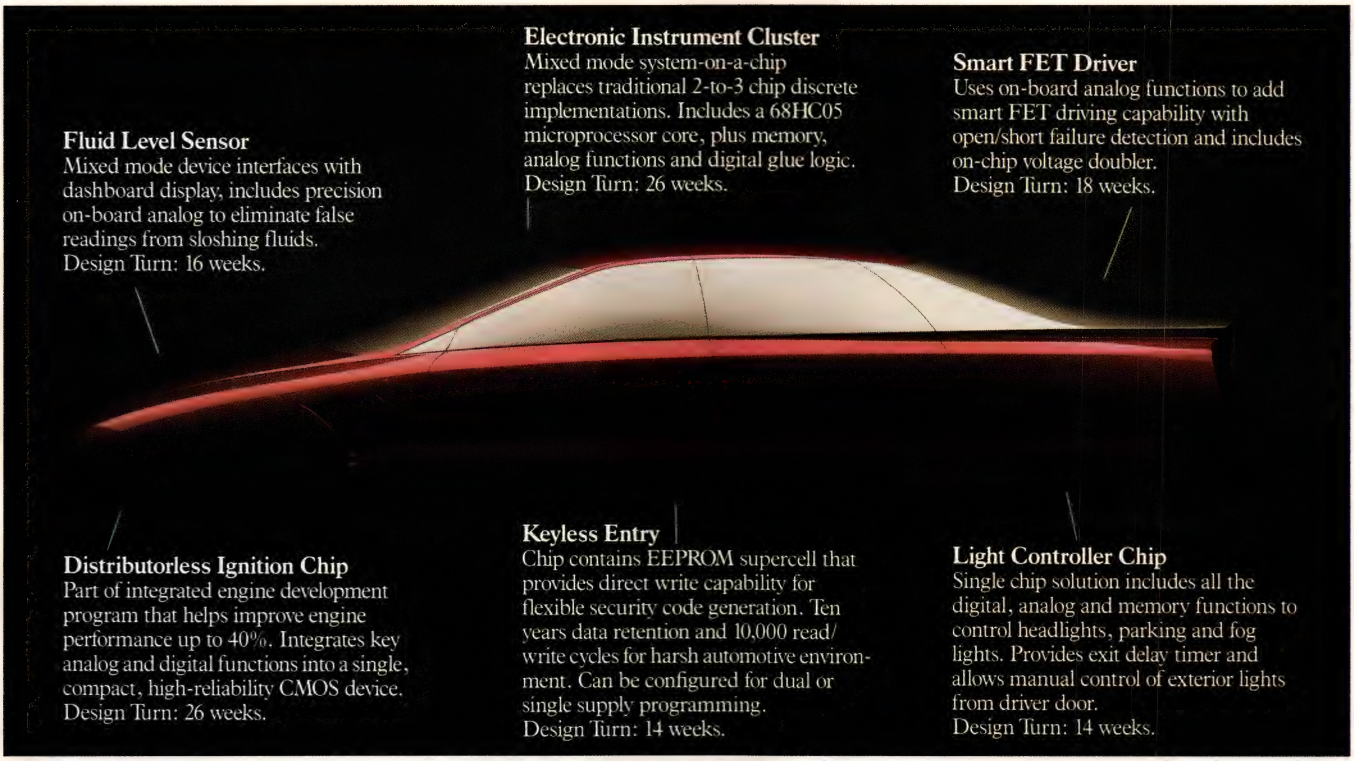


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NCR Microelectronics, 1700 South Patterson Blvd., Dayton, Ohio 45479.

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ory. The debugger works with files created by the vendor's C compiler and assembler, or with any 8051 assembler that can generate output in Intel Hex format. $295.

**Micro Computer Control Corp,** Box 275, Hopewell, NJ 08525. Phone (609) 466-1751. FAX 609-466-4116. TWX 910-240-4881.

**Circle No 401**

## SIMULATOR OPTIONS

- *Let you describe functional blocks to the PSpice simulator*
- *Permit PSpice to do mixed analog/digital simulations*

The Analog Behavioral Modeling option allows you to describe analog components or entire functional blocks to the PSpice simulator. The description can be a formula, a look-up table, a Laplace transform, or a table of frequency response. The transfer function can have any number of controlling variables, including time, and the formula can be as simple or as complex as you wish. This option allows you to describe a functional block by its behavior without having to know how the block will be implemented; at a later stage in the design you can replace the behavioral description by the actual circuitry. The Digital Simulation option allows PSpice to perform mixed analog/digital simulations. The circuit can have any combination of digital and analog signals, and with the aid of the Probe option you can display digital and analog signals simultaneously. The Digital Simulation option includes libraries for most TTL components, and each component includes models for many logic families. The models describe not only the device's functions but also all of the propagation delays. The models are in the form of text files that you can examine or modify. Analog Behavioral Modeling option for an IBM PC running PC-DOS, $350; for a VAX 8800, $4400. Digital Simulation option for an IBM PC running OS/2 or DOS, $1950; for a VAX 8800, $15,900.

**MicroSim Corp,** 20 Fairbanks, Irvine, CA 92718. Phone (714) 770-3022. TLX 265154.

**Circle No 402**

## 1750A TOOL SET

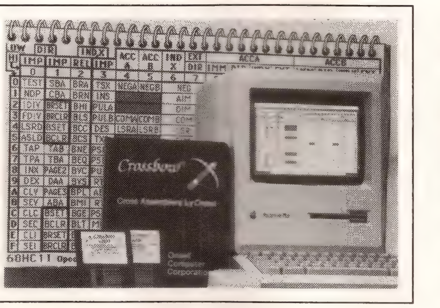
- *Cross-assembler runs on IBM PCs and compatibles*
- *Debugger works with Ada, C, Pascal, or Fortran programs*

The complete 1750A tool set consists of a macro cross-assembler, symbolic debugger, linker, and loader. The macro cross-assembler runs on IBM PCs and compatibles, and generates relocatable object code for MIL-STD-1750A proces-

sors. It can assemble 20,000 lines of source code per minute and offers conditional assembly directives. With only 256k bytes of RAM, it can handle 64 levels of nested subroutines and as many as 16,000 6-character symbols. The linker maps out the target addressing scheme; each of 100 logical groups may link any mix or overlap of program modules. The symbolic debugger runs on the host PC and is therefore nonintrusive; it sports an embedded miniassembler for on-the-spot patches to the program under test. The loader allows the debugger to work on programs written in Ada (or other languages) that run on the target system. Complete tool set, $6845; individual tools also available.

**Sabtech Industries Inc,** 3910-B Prospect Ave, Yorba Linda, CA 92686. Phone (714) 524-3299.

**Circle No 403**



## C CROSS-ASSEMBLER

- *Runs on Macintosh Plus, SE, or II*
- *Generates code for Motorola 6800 and 6300 families of µPs*

Crossbow-6800 is a cross-development package that includes an assembler and a programmer's editor. It runs on a Macintosh Plus, Macintosh SE, or Macintosh II host and assembles code for Motorola 6301, 6800, 6801, and 68HC11 µPs at a rate of 30,000 source-code lines per minute. The built-in editor extends the standard Macintosh editing facilities by adding features such as block- and auto-indenting, independent tab settings, case translation, and comparison of versions in adjoining windows. The assembler provides multifile, conditional, macro, and sectioned-assembly directives. You can direct the assembler to generate object files in Intel Hex format, Motorola S records, or absolute binary code; it optionally creates tabulated source listings and symbol tables. If the assembler finds an error in the source code, it returns you to the editor, places the cursor after the offending word, and explains the nature of the error in a separate window. A built-in communications feature allows you to download the assembler output to a target system at standard transfer rates from 300 to 57,600 bps, using either of the host's serial ports. You can select XON/XOFF handshaking to prevent the target

system's buffers from overflowing during a transfer. You can also perform file transfers under the XModem protocol. $295.

**Onset Computer Corp,** 199 Main St, North Falmouth, MA 02556. Phone (508) 563-2267. FAX 508-563-9477.

**Circle No 404**

## MOTION PROGRAMMER

- *Accepts CAD plotter commands in HPGL format*
- *Converts plotter commands to X-Y motion commands*

SMCCAD is a program that runs on IBM PC/XTs, PC/ATs, and compatibles. It accepts plotter commands in HPGL (Hewlett-Packard Graphics Language) format and converts the commands to constant, programmable-velocity X- and Y-motion commands for the vendor's Smart Motion Control Card (SMCC). The SMCC plugs into an IBM PC expansion slot and can control dc brush, dc brushless, ac induction, and stepping motors. A dynamic buffering feature on the SMCC allows the software to convert a number of moves that are limited only by the available disk space. To run the program, you need 640k bytes of RAM; two 360k-byte floppy-disk drives (or a hard-disk drive if the input drawings are large or intricate); a CGA, EGA, or VGA adapter and color monitor; an SMCC board; and PC-DOS version 2.1 or higher. SMCCAD software, $699; SMCC board, $1199.

**Delta Tau Systems,** 21119 Osborne St, Canoga Park, CA 91304. Phone (818) 998-2095. FAX 818-998-7807.

**Circle No 405**

## COMPONENT LIBRARY

- *Includes more than 600 models of military-qualified parts*
- *Models conform to MIL-M-38510 specification*

The MIL-spec 38510 component library includes more than 600 electronic components qualified for military applications. Each model includes a commercial or ANSI graphical symbol, a precisely characterized simulation model for both functional and timing simulation, and a packaging model for pc-board layout. The library is designed for use with the vendor's line of EDA workstations and software. Five kits are available: TTL, CMOS, ECL, PLD/PLA, and memory components. From $5000 to $10,000, depending on the number and complexity of the parts in the kit.

**Daisy Systems Corp,** Box 7006, Mountain View, CA 94039. Phone (415) 960-6863.

**Circle No 406**

## TEST & MEASUREMENT INSTRUMENTS

### DUAL-DISPLAY DMM

- *Measures two quantities with one pair of leads*
- *Displays two measurements simultaneously*

The model 45 is a 5-digit DMM that sports an unusual dual display. Through one pair of test leads, the meter measures two quantities in rapid succession—for example, a power supply's dc output and rms ripple voltage—and displays both measured values simultaneously. Not only is the dual display unusual, so is the inclusion of a frequency counter, which can measure the frequency of a signal whose rms value is measured by the DMM. The unit incorporates a min/max mode, which records the highest and lowest values attained by a measured quantity. It also includes a relative-measurement mode in which you can store any measured value as a reference and display subsequent readings with respect to the reference. When measuring dc voltage, the unit can resolve 100,000 counts with 0.02%-of-reading inaccuracy at 2.5 readings/sec, 30,000 counts at 5 readings/sec and 3000 counts at 20 readings/sec. An RS-232C port is standard. $595.

**John Fluke Mfg Co Inc,** Box C9090, Everett, WA 98206. Phone (800) 443-5853, ext 33.

**Circle No 410**

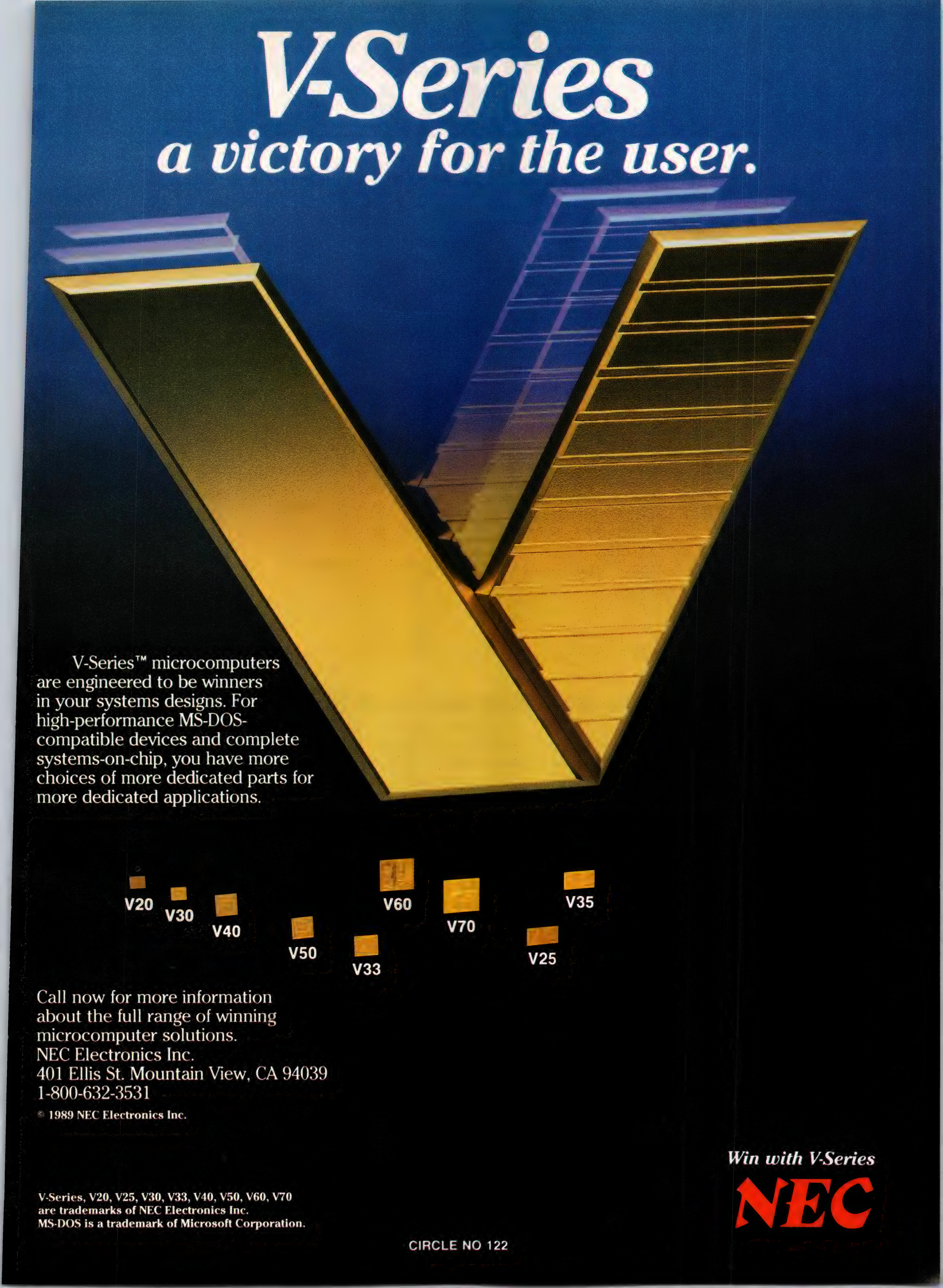
**Philips Test and Measurement,** Building HKF, 5600 MD Eindoven, The Netherlands. Phone local office.

**Circle No 411**

### VXI BUS MODULE

- *Resolves 16 bits on 8 channels*
- *Makes 200k measurements/sec*

The DVX 2502 B-size VXI (VME eXtensions for Instrumentation) module contains an 8-channel data-acquisition system that includes an amplifier whose gain is software programmable and a 16-bit ADC that makes 200,000 conversions/sec.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# MAXIM IMPROVES YOUR ANALOG DEVICES APPLICATIONS

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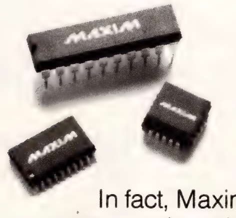

From 1 ppm references to fast 12-bit A/Ds, Maxim offers you the widest selection of *plug-in-replacements* for Analog Devices parts today. They're all available in DIP, SO, or PLCC—at very competitive prices. And, only Maxim makes pin-compatible *improved equivalent* devices like the 3$\mu$s MAX162 that out performs the 5$\mu$s AD7572 in speed and noise. Or, the MAX150 which replaces the AD7820 *and* an external voltage reference.

In fact, Maxim is the *first and only* alternate source for a growing number of Analog Devices parts—such as the AD7534 14-bit DAC, the AD7228 octal voltage output DAC, the AD536A RMS-to-DC converter, the AD7575 5$\mu$s 8-bit ADC with T/H, and more. All Maxim parts are designed to withstand 2000V of electrostatic discharge (ESD), and 50mA of electrical over-stress (EOS). And every DIP is burned-in absolutely FREE.

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### D/A CONVERTERS

| | |
|---|---|
| AD565A | 12-Bit 250ns I-DAC w/Ref |
| AD566A | 12-Bit 250ns I-DAC |
| AD7224 | 8-Bit V-DAC |
| ***AD7225** | **8-Bit Quad V-DAC** |
| AD7226 | 8-Bit Quad V-DAC |
| (MAX500 | 8-Bit Quad Serial V-DAC) |
| ***AD7228** | **8-Bit Octal V-DAC** |
| AD7520 | 10-Bit M-DAC |
| AD7521 | 12-Bit M-DAC |
| AD7523 | 8-Bit M-DAC |
| AD7524 | 8-Bit Latched M-DAC |
| ***AD7528** | **8-Bit Dual M-DAC** |
| (MAX7624 | 8-Bit Latched M-DAC) |
| AD7530 | 10-Bit M-DAC |
| AD7531 | 12-Bit M-DAC |
| AD7533 | 10-Bit M-DAC |
| ***AD7534** | **14-Bit Latched M-DAC** |
| ***AD7535** | **14-Bit Latched M-DAC** |
| ***AD7536** | **14-Bit Latched M-DAC** |
| AD7541 | 12-Bit M-DAC |
| AD7541A | 12-Bit M-DAC |
| AD7542 | 12-Bit Latched M-DAC |
| AD7543 | 12-Bit Serial M-DAC |
| (MAX543 | 12-Bit Serial M-DAC) |
| AD7545 | 12-Bit Latched M-DAC |
| ***AD7545A** | **12-Bit Latched M-DAC** |
| (MAX7645 | 12-Bit Latched M-DAC) |
| AD7548 | 12-Bit Latched M-DAC |
| ***AD7628** | **8-Bit Dual M-DAC** |

### A/D CONVERTERS

| | |
|---|---|
| ***AD578** | **12-Bit 3$\mu$s ADC** |
| ***AD7572** | **12-Bit 5$\mu$s/12$\mu$s ADC** |
| (MAX162 | 12-Bit 3$\mu$s Complete ADC) |
| (MAX170 | 12-Bit 5$\mu$s Serial 8-pin ADC) |
| (MAX172 | 12-Bit Low-Cost 10$\mu$s ADC) |
| AD7574 | 8-Bit 15$\mu$s ADC |
| (MAX160 | 8-Bit 4$\mu$s ADC) |
| ***AD7575** | **8-Bit 5$\mu$s $\mu$P ADC w/S/H** |
| (MAX165 | 8-Bit 5$\mu$s $\mu$P, ADC, S/H, Ref) |
| (MAX166 | 8-Bit 5$\mu$s $\mu$P, ADC, S/H, Ref) |
| ***AD7576** | **8-Bit 10$\mu$s $\mu$P ADC** |
| AD7581 | 8-Bit 8ch 67$\mu$s DAS |
| (MAX161 | 8-Bit 8ch 20$\mu$s DAS) |
| AD7820 | 8-Bit 1.3$\mu$s ADC |
| (MAX150 | 8-Bit 1.3$\mu$s ADC with Ref) |
| ***AD7824** | **8-Bit 4ch 2.5$\mu$s ADC** |
| (MAX154 | 8-Bit 4ch 2.5$\mu$s ADC with Ref) |
| ***AD7828** | **8-Bit 8ch 2.5$\mu$s ADC** |
| (MAX158 | 8-Bit 8ch 2.5$\mu$s ADC with Ref) |

### VOLTAGE REFERENCES

| | |
|---|---|
| AD2700 | +10V, 3ppm Ref |
| (MAX670 | Ultra Precise +10V Ref) |
| AD2710 | +10V, 1ppm Ref |
| (MAX671 | Ultra Precise +10V Ref) |
| AD580 | +2.5V Ref |
| AD581 | +10V Ref |
| AD584 | Programmable Ref |

### THERMOCOUPLE CIRCUITS

| | |
|---|---|
| ***AD594** | **Therm. Amps w/Comp.** |
| ***AD595** | **Therm. Amps W/Comp.** |
| ***AD596** | **Therm. Cond./Cont.** |
| ***AD597** | **Therm. Cond./Cont.** |

### RMS-TO-DC CONVERTERS

| | |
|---|---|
| ***AD536A** | **True RMS-TO-DC Converter** |
| ***AD636** | **Low Level RMS-TO-DC Conv.** |

### V/F AND F/V CONVERTERS

| | |
|---|---|
| VFC32 | Prec. V/F & F/V Conv. |

### AMPLIFIERS

| | |
|---|---|
| AD3554 | Wideband Op Amp |

### MULITIPLEXERS

| | |
|---|---|
| ***AD7506** | **16-CH CMOS Mux** |
| ***AD7507** | **DIFF-CH CMOS Mux** |

* Second sourced only by Maxim

## Send us your application and win an HP27S calculator.

Now that you know how Maxim devices replace or upgrade the Analog Devices parts in your application, send us a schematic or a block diagram detailing how they'd be used.* If, in our humble opinion, your submission is one of the ten best, we'll send you a brand new HP27S calculator! Every entrant will receive a great looking Maxim baseball hat and a 1989 Analog Applications Handbook, so don't delay.

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MAXIM

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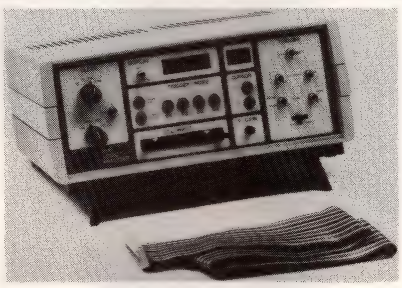
The ADC exhibits no missing codes from 0 to 50°C and allows for internal, external, and data-dependent triggering. The differential inputs have a CMRR >100 dB at 60 Hz. The unit incorporates a 1k-word buffer for the A/D conversion results; the buffer continues to accumulate data during DMA transfers, thus avoiding gaps in the acquired data. The sequence controller, which includes a precision clock, can store such information as the correct gain and trigger mode for each channel. $3700. Delivery, eight to 10 weeks ARO.

**Analogic Corp,** 8 Centennial Dr, Peabody, MA 01961. Phone (800) 343-8333; in MA, (508) 977-3000. TLX 949307.

**Circle No 412**



## LOGIC ANALYZER

- *Converts your scope into 16-channel analyzer*
- *Has clock with four speeds to 10 MHz*

You can connect the 3.75-lb, 4×7×10-in. LA-1610 logic analyzer to an oscilloscope. When you've set the scope's sensitivity to 0.5 V/div and its sweep speed to 50 µsec/div, you've converted the scope into a 16-channel logic analyzer that can capture 256 events and display 32 of them at once on the scope's screen. You can also position a cursor and read the data on a set of six 7-segment LEDs. You can qualify the trigger conditions in several ways; for example, by setting specific values for the incoming data. You can use the unit as a timing analyzer; it has an internal clock

# TEK BRINGS FFT ANALYSIS OUT OF THE DARK AGES.

See the light. With the Tektronix 2630 Fourier Analyzer.

**See the light with power.** Used as a smart terminal, your PC can unleash the incredible power of the 2630 through high-quality graphics, full keyboard control and nearly limitless mass storage.

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Step out of the Dark Ages into the light with the 2630 Fourier Analyzer. And never look back. For details, or to receive a demo disk, call 1-800-234-1256, or write: Tektronix, 1350 Dell Ave., Suite 104, Campbell, CA 95008.

## The 2630 *Personal* Fourier Analyzer

---

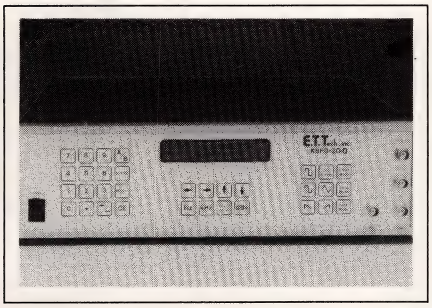


**Tektronix**®
COMMITTED TO EXCELLENCE

whose rate you can set to four values from 1.25 to 10 MHz. $495.

**Global Specialties,** Box 1405, New Haven, CT 06405. Phone (800) 634-0762; in CT, (800) 445-6250. FAX (203) 468-0060.

**Circle No 413**



## 20-MHz GENERATOR

- *Produces synthesized quadrature outputs*
- *Resolves frequencies to six digits*

The KSG-20Q is an IEEE-488-controlled 0.1-Hz to 20-MHz frequency synthesizer and function generator. It has a pair of outputs related in phase by 90° that can deliver 20V p-p into a 50Ω load. The output amplifiers can slew at 1.5V/nsec; they follow attenuators that you can program over a 60-dB range. Six-digit resolution lets you increment the output frequency in steps of μHz at the lowest frequency and several Hz at the highest frequency. An LCD indicates the output voltage in dBV or V p-p and the frequency. The unit stores several front-panel setups. $2245; KSG-20 (with single output), $1845.

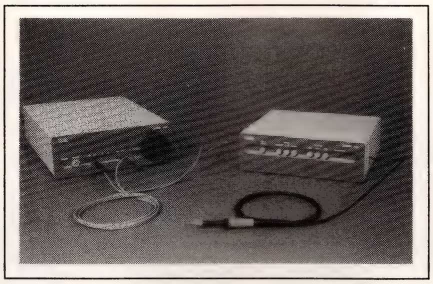
**ET Tech Inc,** 15 S Van Brunt St, Englewood, NJ 07631. Phone (201) 569-3339. TLX 642145.

**Circle No 414**

## SCOPE ISOLATOR

- *Measures at CMV limited only by fiber-optic cable*
- *Provides 15-MHz bandwidth (−3dB)*

The Isobe 3000 is a wideband fiber-optic isolator for off-ground analog signals that you need to display on



a scope. The isolator consists of two units—a battery-powered transmitter and a receiver. The properties of the fiber-optic cable impose the only real limit on the permissible common-mode potential between the transmitter and the receiver. Though the spec is 100 dB to 10 kHz, the CMRR at dc is essentially infinite. The isolator is dc coupled and has a −3-dB bandwidth of 15 MHz. With 1m cable, $2495; with 50m cable, $2795.

**Nicolet Instrument Corp,** Box 4288, Madison, WI 53711. Phone (800) 356-3090; in WI (608) 271-3333. TWX 910-286-2737.

**Circle No 415**

## BENCHTOP SUPPLY

- *Provides two 0 to 30V and one 4 to 6V output*
- *Includes a tracking output facility*

The TS3023S is a triple-output benchtop power supply. Two of its outputs provide as much as 2A at voltages in the range 0 to 30V, and the third output provides as much as 4A at 4 to 6V. All the unit's outputs feature remote-sensing terminals. The 2A, 0 to 30V outputs each have two 3½-digit LCDs that simultaneously display both the output current and voltage. With the corresponding output switched off, you can use these displays to preset the output voltage and the output current limit prior to connection of a load. These outputs also have coarse and fine voltage controls that allow you to set the output voltage at a resolution higher than 5 mV. Their current-limit control is logarithmic to ensure adequate control


# The program in a switch.

Introducing Vivisun Series 2000, the programmable display pushbutton system that interfaces the operator with the host computer. The user friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence, such as a checklist, with no errors and no wasted time.

They also simplify operator training as well as control panel design. Four Vivisun Series 2000 switches can replace 50 or more dedicated switches and the wiring that goes with them. In short, Vivisun Series 2000 gives you more control over everything including your costs.

Contact us today.

**AEROSPACE OPTICS INC.**
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 · Telex 75-8461 · Fax (817) 654-3405

SERIES
# VIVISUN 2000™

*Programmable display switches. Making the complex simple.*

CIRCLE NO 159

at low current settings. They automatically cross over from constant voltage to constant current mode, and a display annunciator indicates when the constant current mode is active. You can switch the two 0 to 30V outputs into a tracking mode. The 4A, 4 to 6V output has a single 3½-digit LCD that displays the output voltage when the output is switched off, and the output current when the output is on. All the outputs are protected against both forward and reverse voltages. £385.

**Thandar Electronics Ltd,** 2 Glebe Rd, Huntingdon, Cambridgeshire PE18 7DX, UK. Phone (0480) 412451. TLX 32250. FAX 0480-411463.

**Circle No 416**

## VLSI TESTERS

- *Burst 200M patterns/sec without multiplexing*
- *Drive and sense on 256 and 512 pins*

The LT-1001 and the LT-1101 are 256-pin and 512-pin testers, respectively, for VLSI devices. Except for pin count, the systems provide identical electrical performance. The I/O channels have a voltage range of −2.5 to +7.5V. They drive the DUT (device under test) from a 50Ω source and load the DUT with 50Ω. According to the vendor, these impedance and voltage levels, coupled with a nonmultiplexed 200M pattern/sec data rate, allow the systems to test ECL, high-speed TTL, and CMOS parts and also allow single-pass testing of BiCMOS and BiMOS devices. The systems combine shared resources with tester-per-pin architectural concepts. LT-1001, $1,200,000; LT-1101, $2,300,000. Delivery, 90 days ARO.

**Tektronix Inc,** Box 4600, MS 94-441, Beaverton, OR 97076. Phone (503) 629-1035.

**Circle No 417**

# A.T.E.


# P.D.Q.

## Keithley's 556 adapts to your tests as fast as you can change cards.

If your automated test requirements change often, you know how difficult it is to keep up. Expensive new instruments. Sensors that require special conditioning. Complex programming.

Not any more. Now the Keithley Model 556 GPIB Measurement & Control System lets you interface a full range of transducers to the IEEE-488 bus. Mix any 10 signal conditioning modules from a library of over 25 specialized functions. Thermocouples, strain gages, digital and analog I/O, power control, frequency, motion . . . more.

Simple yet powerful commands run with the language of your choice, and work with Mac, NEC, DEC, HP, or any 488 controller. On-board intelligence and memory let the 556 run as a stand-alone datalogger or process controller.

Best of all, this power and performance start around $2500. Check it out, PDQ, with a toll-free call to the PC Team at **1-800-552-1115.** Or write: Data Acquisition & Control Division, Keithley Instruments, Inc., 28775 Aurora Rd., Cleveland, OH 44139.

GPIB IEEE-488

KEITHLEY

CIRCLE NO 37

digelec *PROM & Logic Programmers*

# 1-2-3-4 AT A TIME MAKES PROGRAMMING AS EASY AS 1-2-3-4

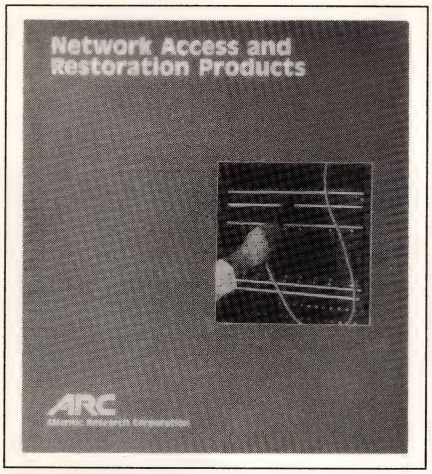

**MODEL 825**
**SET PROGRAMMER**

- **PROGRAMS:**
  - ☐ Up to 4 devices simultaneously with the **same** or **different** data.
  - ☐ **16K to 1024K** Bit **E²/EPROMs** from all manufacturers (more than 220 devices)
  - ☐ **Intel (87 xx)** and **Motorola (68701/68705,** 28- and 40-pin) **single-chip micros**
- **FEATURES:**
  - ☐ **8, 16, 32** bit or **GANG** operations
  - ☐ **64K Byte** standard **RAM** (expandable to **256K Byte)**
  - ☐ **Built-in UV eraser**
  - ☐ Plug-in **SOFTPACK** cassette for do-it-yourself software updates
  - ☐ Programming **Verification at 3 VCCs**
  - ☐ Fully **programmable VCC & VPP** for future programming needs
  - ☐ **Detects Device type** (signature)
  - ☐ **Detects misplaced** device
- **SUPPORTS:**
  - ☐ 5 different programming algorithms, including **Intel Intelligent** and **Quick-Pulse, AMD Flashrite**
- **OFFERS OPTIONALLY:**
  - ☐ **SOFTLINK** remote control software for **IBM PC/XT/AT**
  - ☐ **PLCC** module
  - ☐ Adapter for **1 M bit EPROMs** and **Motorola micros**

digelec

**USA: DIGELEC INC.,**
22736 Vanowen Street
Canoga Park, CA 91307
Tel: (800) 367-8750
In CA: Tel: (818) 887-3755
Fax: (818) 887-3693

CIRCLE NO 36




## Brochure presents network-access products

This 24-pg brochure describes the vendor's complete line of network-access and restoration products. The booklet covers digital, VF, and coaxial patching and switching equipment; interface converters; the Restorer multiline dial-backup system; NTS network management systems for data; the Artacs PBX Management system for voice; and Interview Series test instrumentation.

**Atlantic Research Corp,** Teleproducts Div, 7401 Boston Blvd, Springfield, VA 22153.

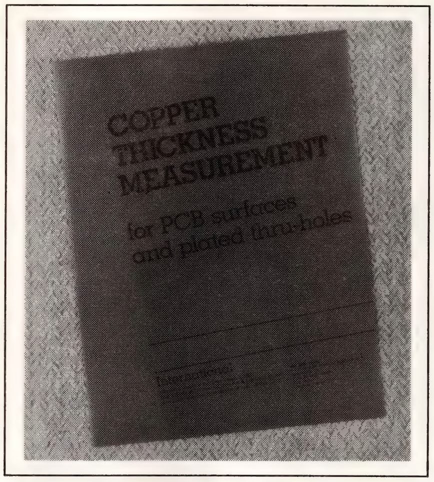
**Circle No 420**

## Study reports on user ratings of equipment

The vendor's annual computer-user survey "US User Ratings of Mainframes and Minicomputers" polls more than 1100 mainframe and minicomputer users. The 40-pg study combines data about systems and usage with user ratings of equipment and manufacturer support and provides an evaluation tool for prospective users of computer systems. Current users discuss their system's hardware configuration, organization, price, and planned expansions. Additional questions cover specific reasons for customer satisfaction, such as ease of operation, system or peripheral reliability, maintenance service, technical support, ease of programming and conversion, and overall satisfaction. $200.

**Datapro Research,** 1221 Avenue of the Americas, New York, NY 10020.

**INQUIRE DIRECT**




## Modular system for measuring pc-board copper

This 4-pg brochure introduces the MR 4000 modular-coating thickness-measuring system that helps you select the components that are most suitable for pc-board surface-copper or plated through-hole quality-control requirements. The publication provides complete component specifications and a list that explains the functions of each component. Further, it specifies two statistical packages, standard and "Stats-Plus" for customized header software.

**CMI International,** 2301 Arthur Ave, Elk Grove Village, IL 60007.

**Circle No 421**

## Comprehensive listing of power supplies

The vendor's 1989 catalog lists more than 150 new power supplies and dc converters. The 200-pg publication lists products that come in commercial, industrial, and military versions. Other sections of the 9-part catalog deal with laboratory and test equipment, custom power

# Make your move to P&B for new general purpose and power P.C. board relays.


**New Models Expand Offering**

For applications from consumer goods to industrial controls, P&B relays have the features you need for general purpose and power switching on your printed circuit board. New series greatly expand our already broad line of P.C. board relays. Many models are available from stock, and they're all built to the same exacting standards that have made our T90 series the industry-standard 30A, P.C. board relay.

**New Miniature Relays Switch 1mA to 10A**

Our new T73 and T74 series miniature P.C. board relays join the T70 series as inexpensive SPDT units for general purpose applications. A variety of contact materials allow units in these series of sealed relays to switch loads from 1 mA through 10A.

**Expanded Line of 4,000V Isolation Relays**

Extensions to our line of RK series relays feature 8mm coil-to-contact spacing for 4,000V isolation. SPDT models switch loads to 20A, and DPDT models switch up to 5A. Both sealed and unsealed types are offered.

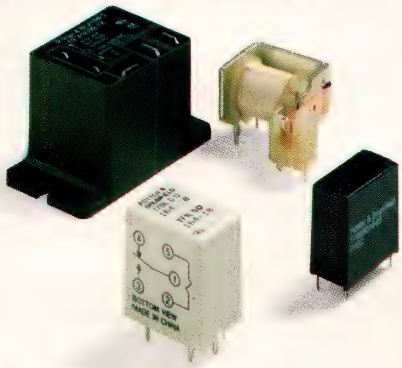
**T90 & T91 — Our 30A Workhorses**

Relays in our T90/T91 series have SPDT contacts for loads to 30A. T90 is available as a sealed or open-style relay. T91 has quick connect terminals for load connections and is offered with either a sealed or unsealed enclosure. High temperature units are available.

**Find Out More**

Contact us today for free information on the complete line of P&B P.C. board relays, including more new models for switching 2A and less. Potter & Brumfield, A Siemens Company, 200 S. Richland Creek Drive, Princeton, Indiana 47671-0001.

**Call toll-free 1-800-255-2550 for the P&B authorized distributor, sales representative or regional sales office serving your area.**



Potter & Brumfield A Siemens Company



8703A

systems, and accessories. A product selector guide, a section of mechanical drawings, and warranty and ordering information complete the catalog.

**Lambda Electronics,** 515 Broad Hollow Rd, Melville, NY 11747.

**Circle No 422**

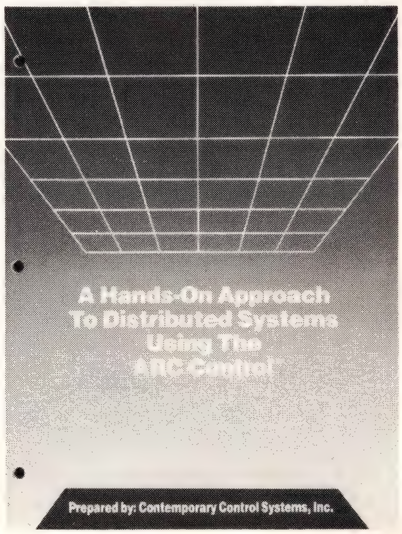
## Supplement for microwave test accessories

In this 20-pg supplement to the 1986 catalog, the vendor describes the latest coaxial and waveguide-measurement accessories. The publication features the 2.4-mm coaxial connector and products such as detectors, attenuators, and terminations. Also highlighted are mm-wave waveguide products that range from 26.5 to 110 GHz and include precision coupler/attenuators, mismatches, and terminations. The publication notes that the recent introduction of new vector and scalar network analyzers has generated a need for updated calibration and verification kits to support these instruments. A current index provides a list of discontinued products.

**Hewlett-Packard Co,** 19310 Pruneridge Ave, Cupertino, CA 95014.

**Circle No 423**

## Discussion of distributed control systems




*A Hands-On Approach to Distributed Systems Using ARC Control* discusses the design and application of ARC Control, an IBM PC or compatible bus-based intelligent I/O subsystem. The 74-page handbook provides figures, photos, and tables and concludes with four appendixes containing an acronym guide, answers to ARC-control questions, references, and a component list that provides power-consumption requirements.

**Contemporary Control Systems Inc,** 2500 Wisconsin Ave, Downers Grove, IL 60515.

**Circle No 424**

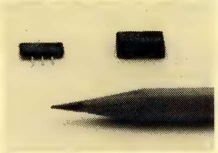
# EDN PRODUCT MART

**This advertising is for new and current products.**

**Please circle Reader Service number for additional information from manufacturers.**

## ELMEC — ULTRA HIGH-SPEED FIXED DELAY LINES

**FDC TYPE SINGLE IN LINE** — **FDR TYPE SURFACE MOUNT**



FDC and FDR types can be fully matched to high speed logical elements such as 100K, 10KH and 10K series and has an extensive range of applications including analog circuit.

| Part Number: Single In | Part Number: Surface Mount | Impedance | Delay Time | Output Rise Time (20%–80%) | Pass Band −3dB |
|---|---|---|---|---|---|
| FDC 0505 | FDR 0505 | 50Ω ± 10% | 0.5ns± 0.10ns | 300ps or Less | 800MHz or More |
| FDC 1005 | FDR 1005 | | 1.0ns± 0.10ns | 300ps or Less | 800MHz or More |
| FDC 1505 | FDR 1505 | | 1.5ns± 0.15ns | 400ps or Less | 550MHz or More |
| FDC 2005 | FDR 2005 | | 2.0ns± 0.20ns | 400ps or Less | 550MHz or More |
| FDC 2505 | FDR 2505 | | 2.5ns± 0.20ns | 500ps or Less | 450MHz or More |
| FDC 3005 | FDR 3005 | | 3.0ns± 0.20ns | 500ps or Less | 450MHz or More |
| FDC 3505 | FDR 3505 | | 3.5ns± 0.25ns | 600ps or Less | 400MHz or More |
| FDC 4005 | FDR 4005 | | 4.0ns± 0.30ns | 700ps or Less | 350MHz or More |
| FDC 4505 | FDR 4505 | | 4.5ns± 0.30ns | 700ps or Less | 350MHz or More |
| FDC 5005 | FDR 5005 | | 5.0ns± 0.30ns | 700ps or Less | 350MHz or More |
| FDC 0510 | FDR 0510 | 100Ω ± 10% | 0.5ns± 0.10ns | 300ps or Less | 800MHz or More |
| FDC 1010 | FDR 1010 | | 1.0ns± 0.10ns | 300ps or Less | 800MHz or More |
| FDC 1510 | FDR 1510 | | 1.5ns± 0.15ns | 400ps or Less | 550MHz or More |
| FDC 2010 | FDR 2010 | | 2.0ns± 0.20ns | 400ps or Less | 550MHz or More |
| FDC 2510 | FDR 2510 | | 2.5ns± 0.20ns | 500ps or Less | 450MHz or More |
| FDC 3010 | FDR 3010 | | 3.0ns± 0.20ns | 500ps or Less | 450MHz or More |
| FDC 3510 | FDR 3510 | | 3.5ns± 0.25ns | 600ps or Less | 400MHz or More |
| FDC 4010 | FDR 4010 | | 4.0ns± 0.30ns | 700ps or Less | 350MHz or More |
| FDC 4510 | FDR 4510 | | 4.5ns± 0.30ns | 700ps or Less | 350MHz or More |
| FDC 5010 | FDR 5010 | | 5.0ns± 0.30ns | 700ps or Less | 350MHz or More |

**ELMEC TECHNOLOGY OF AMERICA, INC.** 1225 Ridgecrest St., Monterey Park, CA 91754
Phone: (213) 265-1861 FAX: (213) 265-1908

**CIRCLE NO 325**

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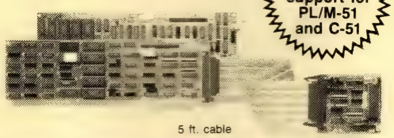
☆ ☆ ☆ ☆

*"The Best 8051 Emulator"*

**NEW** Source Level support for PL/M-51 and C-51



5 ft. cable

# 8051

*See EEM 88/89 Page D-1304*

**PC based emulators for the 8051 family**

**(8051/51FA/52/31/32/44/152/451/452/535/552 + CMOS + more ...**

- PC plug in boards or RS-232 box
- Pull-down menus combined with Command-Driven User Interface. Context sensitive help and On-Screen Editing of data
- 20 MHz real time emulation
- 128K emulation memory
- 48 bit wide, 16K deep trace buffer with loop counter
- Program Performance analyzer
- Powerful Macros with IF-ELSE, REPEAT-WHILE structures
- Source Level debug for PL/M-51 and C-51
- Symbolic debugging with in-line assembler and disassembler
- Execution time counter
- Trace can be viewed during emulation!

**PRICES: 32K Emulator for 8031 $1790;* 4K Trace $1495***

**CALL OR WRITE FOR FREE DEMO DISK!**

***Ask about our demo VIDEO!***

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**NOHAU CORPORATION** 51 E. Campbell Avenue, Campbell, CA 95008, FAX (408) 378-7869, **(408) 866-1820**

**CIRCLE NO 326**

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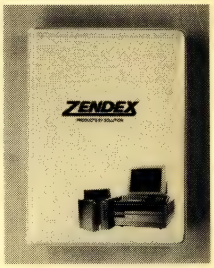
## FREE CATALOG!

**MULTIBUS BOARD PRODUCTS MULTIBUS I, II & VME ENCLOSURES**




**1989 36 Page Catalog features:**

- ZX-286 PC/AT CPU
- ZX-286/20 20MHz CPU
- ZX-386/16 CPU
- ZX-298 SCSI Host Adapter w/Clock
- ZX-981 Universal Enclosure

**ZENDEX**

6700 Sierra Lane, Dublin, CA 94568
TEL: (415) 828-3000 FAX: (415) 828-1574

**CIRCLE NO 327**

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## FREE SCHEMATIC CAPTURE DEMO DISK

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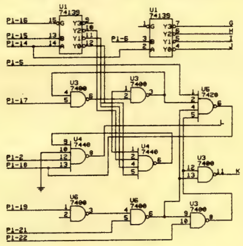

Incredible speed, ease of use and power have made SCHEMA a best-selling schematic capture program for engineering professionals the world over. Now, SCHEMA II+ sells for **$495** and supports most common IBM PC/XT/AT/PS2 configurations.

**OMATION**

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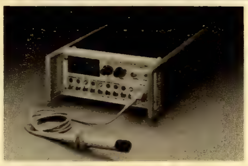

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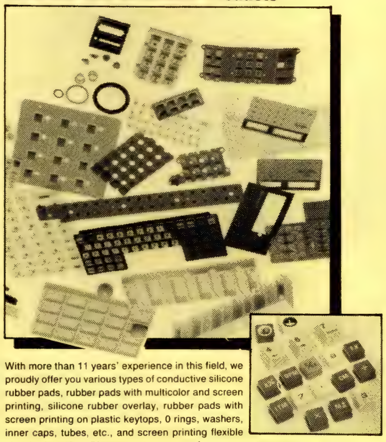

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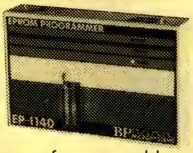


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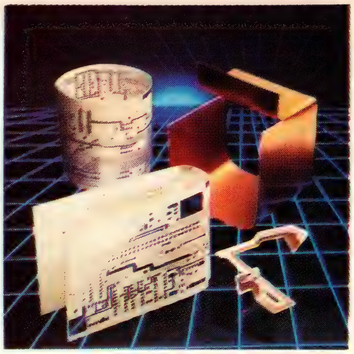

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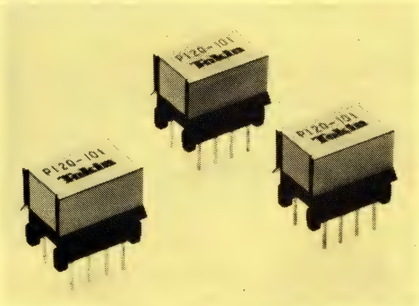


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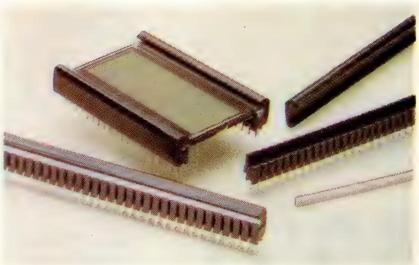

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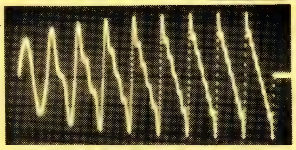

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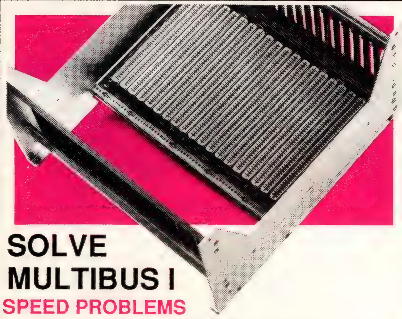

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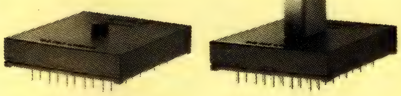

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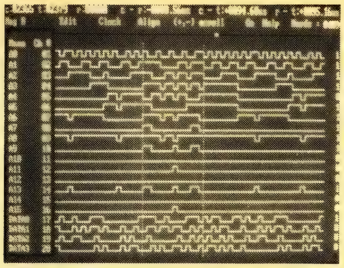

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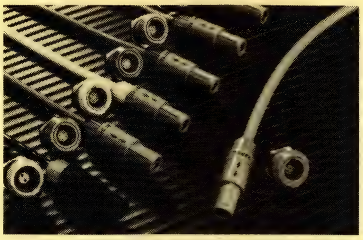

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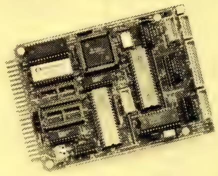

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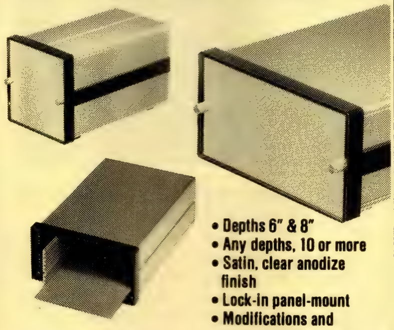

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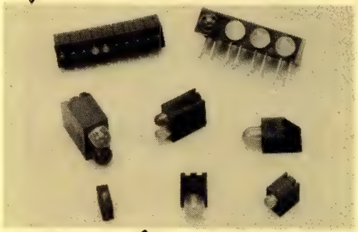

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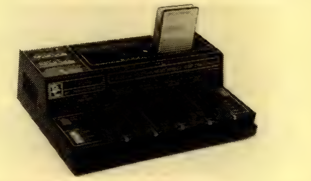

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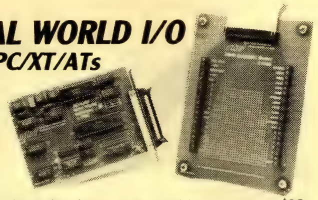

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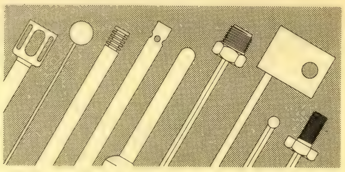

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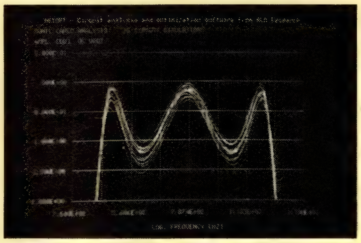

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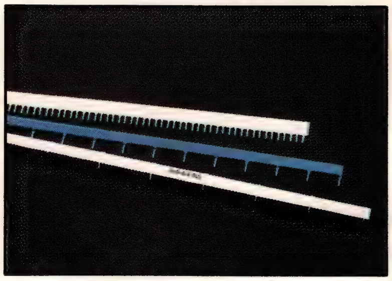

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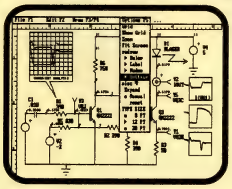

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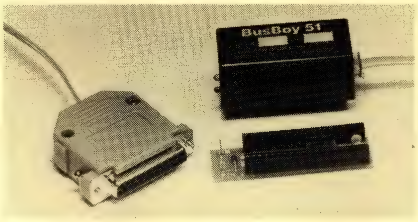

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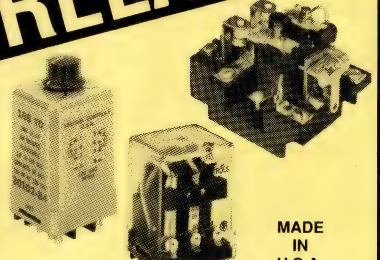

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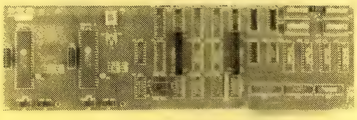

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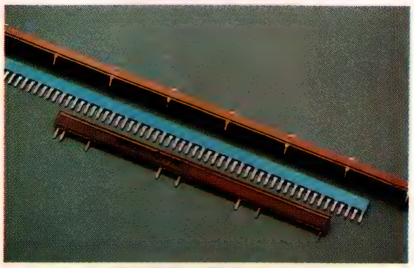

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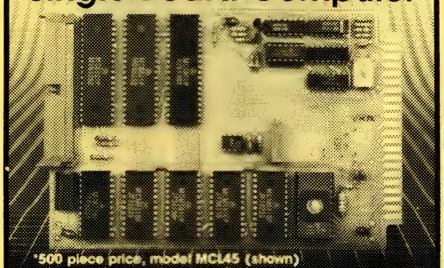

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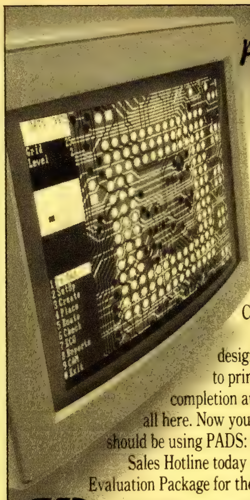

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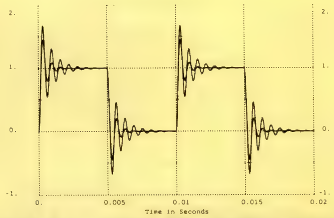


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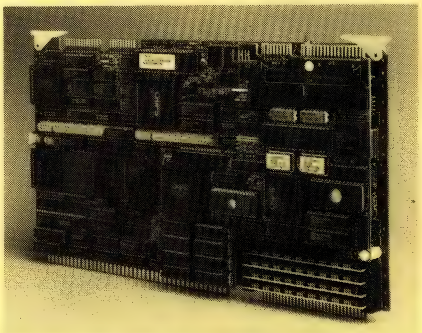

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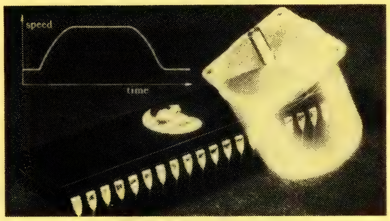


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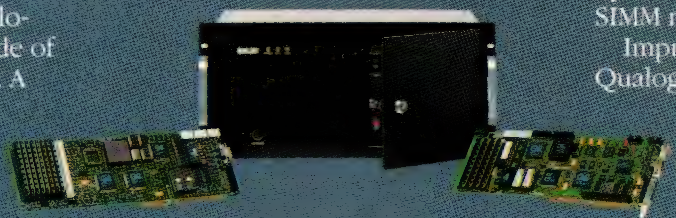

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# Improving working conditions for engineers: Should the IEEE do more?

**Paul Kinnucan**

The free market structure that characterizes the US economy tends to create a tussle between engineers and employers over salaries, benefits, job security, discrimination, and other career-related issues. Fortunately, electrical and electronics engineers have a potentially powerful ally when confronting employers with such issues—the Institute of Electrical and Electronics Engineers (IEEE), the world's largest engineering society.

The New York City-based society, which comprises 304,000 members worldwide in 754 chapters, works to improve the professional lives of engineers. According to Edward Bertnolli, IEEE vice-president of professional activities, the IEEE's goals range from providing members with information on salaries, pensions, and patent rights to pressing Congress for tax and pension reform legislation.

Despite these efforts, some members believe that the IEEE isn't doing enough to resolve the many problems that plague today's engineering profession. They want the society to devote more of its $82 million annual budget and 500 full-time staff members to improving work conditions and pursuing a wider range of legal issues. In the past, the IEEE


Kevin Hawkes

Though the IEEE originally functioned as a technical society, it now works to provide its members with information on salaries, job opportunities, pensions, and legal rights.

has responded to such demands for more career-related support—though few members have rallied as vehemently as some of today's critics.

The IEEE originally functioned as a purely technical society and gradually became the career-conscious institution it is today. Formed in the 1950s by the merger of several societies, some of which date back to the late 19th century, the IEEE worked to improve and broaden the applications of what it terms "electrotechnology." To educate its members, the society created numerous technical journals (including its flagship publication, the *IEEE Spectrum*), conferences, and technical standards.

**The IEEE changes direction**

In the 1960s, however, the society came under increasing pressure to address the career-related concerns of its members. Such pressure became especially intense in the early 1970s when many members were put out of work because of the recession in the US aerospace industry. At that time, the US members voted to have the IEEE devote its resources to improving working conditions for electrical and electronics engineers.

The IEEE created a US Activities Board (USAB) in 1972 to direct the society's activities and provide the support its members requested. The USAB, based in Washington, DC, also oversees another IEEE initiative—developing and presenting IEEE positions on US technology policy.

Today, the USAB comprises 20 full-time staff members and commands a \$2.7 million annual budget. To help IEEE members understand and deal with the current issues in the industry, the USAB offers both professional and legal assistance.

The group gathers and publishes a range of information that can help engineers to improve salaries, benefits, and working conditions. For example, the USAB issues an annual membership salary survey and booklets on pensions, patent rights, age discrimination, and professional ethics.

Each year, the USAB sponsors workshops and conferences on the status of engineering careers. These meetings let IEEE's members and managers and employers exchange information and views on engineering career-related issues, such as pensions, patent rights, and age discrimination. In addition, the USAB maintains speakers bureaus that list members who are willing and qualified to speak on these issues.

The USAB also sponsors electronic registries of members who are actively seeking work. Potential employers may search the database to find qualified candidates. To protect the employed registrants, the companies that operate the registries never divulge registrants' names to prospective employers. Instead, registrants are notified when potential employers express an interest in them. The registrants can then contact the prospective employers. Currently, the USAB sponsors two registries, one for company-employed registrants (PEER) and one for self-employed registrants (SEER).

**Justice for all members**

In addition to heightening the members' awareness of career-related issues and simplifying their job search, the USAB tries to improve working conditions by providing legal guidance. The group appears before Congress regularly to support legislation that might benefit its members and to oppose

legislation that might harm members. In the late 1970s, for example, the USAB successfully lobbied in support of legislation that established Individual Retirement Accounts (IRAs). Such accounts, in effect, let employees create their own pension funds—a valuable benefit to engineers who, because of high job mobility, often don't stay long enough with an employer to benefit from company-sponsored plans.

The society's current lobbying agenda includes support for:

- Establishing portable pensions, which allow employees to transfer their pension assets from one company's plan to another when changing jobs
- Outlawing integrated pensions, whose benefits are offset by the employee's Social Security benefits
- Requiring companies to adopt defined-contribution pension plans, which protect employees' pension benefits from the ravages of inflation
- Repealing a provision (Section 1706) in the 1986 tax reform act that eliminated certain tax benefits for self-employed engineers
- Providing a cooling-off period for employees who accept early retirement in return for a compensation package (golden handshake) and
- Allowing early retirees to sue their former employers for improved compensation even if the retirement agreement includes a no-sue provision.

To magnify its influence on Congress, the USAB always tries to ally itself with other groups that have interests on similar issues, Bertnolli says. Last year, for example, the USAB appeared before Congress with the American Association of Engineering Societies to support legislation that would pave the way for portable pensions. Bertnolli points out that the joint lobbying effort represented nearly 1½ million engineers before Congress.

The USAB confronts other government organizations to protect the interests of its members. For example, the USAB will lobby the Defense Dept intensively this year to push for legislation that will make it illegal for defense contractors to use mandatory uncompensated overtime as a way of lowering their bids.

In addition to lobbying for new legislation, the USAB monitors the enforcement of current laws and regulations. The group tracks the performance of an agency responsible for enforcing a Federal law against age discrimination. It also monitors employment advertisements for evidence of age discrimination and advises companies that violate the law.

If IEEE members are directly affected by such legal violations, the society often takes court action. The USAB has a long-standing policy of testifying on behalf of members in age-discrimination and ethics cases as a "friend of the court." Several years ago, for example, the society took part in an ethics case involving members who worked on the design of San Francisco's Bay Area Rapid Transit (BART) system.

### Too little, too late

Despite the IEEE's declared dediction to these causes, the society hasn't escaped criticism. Irwin Feerst, a member and perennial IEEE presidential candidate, questions both the scope and the vigor of the IEEE efforts. Feerst claims, for example, that the society

Critics claim that the IEEE needs to broaden its current agenda of career-related activities and pursue its lobbying efforts more vigorously.

doesn't monitor Congress closely enough and therefore misses opportunities to lobby for important engineering issues.

Feerst would like to see the IEEE expand its current legislative agenda signficantly. Regarding patent rights, for example, Feerst wants the IEEE to press for legislation that would entitle engineers to 25% of the royalties gained by a company as a result of the engineer's patented work. The IEEE, however, currently supports most companies' position that the ideas and products developed by an engineer should belong to the company that currently employs the engineer.

Feerst's major criticism of the IEEE is that it doesn't strike at the root of what he believes is the cause of most of the professional problems facing US engineers—an oversupply of engineering talent. "There is a huge glut of engineers in the US today," Feerst declares.

According to Feerst, this oversupply has made it difficult for many engineers, especially older engineers who are more expensive than younger engineers to employ, to find work. Furthermore, those engineers who do find work can't always negotiate for improved salaries, benefits, and working conditions.

### A question of degree

Feerst urges the IEEE to actively discourage young people from entering the engineering profession by publicizing this issue and its harmful consequences. To reduce the engineering population, he also advocates banishing anyone from the IEEE who has a bachelor of engineering technology (BET) degree. Companies are eager to hire such persons, whom Feerst terms "subprofessionals," because they command a lower salary than individuals with an EE degree. The IEEE aids these potential competitors of EEs by conferring membership on them, Feerst claims.

In addition to suggesting that the IEEE tighten its membership requirements, Feerst advises the society to support legislation that would make it illegal for US companies to employ non-nationals as electrical engineers. Because such engineers are often willing to work for extremely low wages, they decrease the job opportunities available for engineers who are US citizens, Feerst says.

Although Feerst has advocated these measures for years, he has thus far made little headway in gaining support from the IEEE hierarchy, which selects the specific professional issues that the organization will address. Support hasn't been forthcoming, Feerst says, because these measures oppose the interests of the IEEE hierarchy, which is composed primarily of academics and corporate executives. He believes that academics have a natural interest in encouraging young people to enter the engineering profession. Similarly, he asserts corporate executives want to have a large pool of engineering talent from which to draw.

The IEEE hierarchy, however, cites different reasons for refusing to support Feerst's proposals. It disagrees with Feerst's premise that there is an oversupply of engineers, according to USAB chairman Bertnolli. In fact, the IEEE maintains that dropping enrollment in US engineering schools could precipitate a critical shortage in engineering talent. Such a shortage could put US companies at a serious disadvantage in competing against companies based in other countries, notably Japan, that have a large engineering force. For this reason, the IEEE is increasing its efforts to encourage students to choose engineering as a profession by providing speakers and video tapes for school functions, Bertnolli says.

Finding the IEEE hierarchy unresponsive to his views on professional issues, Feerst has long sought to unseat that hiearchy through the IEEE electoral process. He hasn't been successful at attaining his desired position of authority, but Feerst has managed to circulate his views throughout the engineering industry. Although IEEE members probably won't see any drastic changes in the society's agenda in the near future, they may begin to reevaluate their satisfaction or discontent with the society's efforts to improve the professional lives of engineers. EDN

### Author's biography

*Paul Kinnucan, a Boston-based freelance writer, specializes in electronics, computer, and aerospace-related topics.*

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| June 8 | May 18 | Components,<br>Digital ICs | |
| June 22 | June 1 | Semicustom ICs,<br>Computer Boards | Closing: June 9<br>Mailing: June 29 |
| July 6 | June 15 | Product Showcase —<br>Volume I, Power Supplies | Closing: June 22<br>Mailing: July 13 |
| July 20 | June 29 | Product Showcase —<br>Volume II, Components | Closing: July 21<br>Mailing: Aug. 10 |
| Aug. 3 | July 13 | Integrated Circuits,<br>Computer Boards | |
| Aug. 17 | July 27 | Military Electronics Special Issue<br>Military Software | Closing: Aug. 4<br>Mailing: Aug. 24 |
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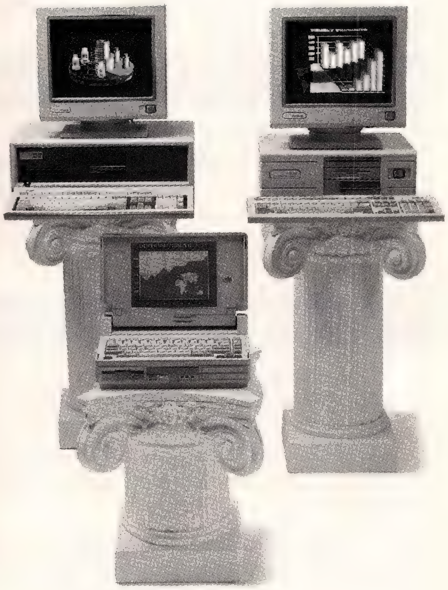

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EDITED BY JULIE ANNE SCHOFIELD

## Consumers are unaware of fax for personal computers

Personal-computer facsimile boards have been around since 1985, but many telecommunications and management-information-system experts are unaware of them, according to an industry report by Venture Development Corp (Natick, MA). This low level of awareness might discourage some manufacturers, but it could also help them form new marketing strategies.

These boards enable personal computers to act as facsimile transceivers, but buyers of personal-computer fax boards see them as additions to stand-alone facsimile machines, not as replacements for them. Of the owners VDC surveyed, 58.3% said that the same individual or department purchased both stand-alone facsimile machines and personal-computer fax boards. Most of the owners usually order the stand-alone units from local dealers, but 81% of personal-computer fax-board users ordered their boards directly from the manufacturer. VDC expects this figure to decrease as more computer dealers offer these boards.

The most important factor for first-time buyers was the compatibility of the board with the other facsimile equipment in their office, and many buyers want to be able to test personal-computer fax boards at their site. Reliability, transmission speed, copy quality, ease of use, and price also heavily influenced buyers. The average price for a personal-computer fax board is $500, reports VDC.

Half of the companies that have personal-computer fax boards own only one unit, 19% own two, and 31% own three or more. Nearly half of the owners surveyed by VDC plan to buy more boards over the next five years.

## NASA information-systems budget to increase to $1.3B

The market for contracted information systems and services in the National Aeronautics and Space Administration (NASA) will increase from $910 million in 1988 to $1.3 billion by 1993, predicts Input (Mountain View, CA). This figure represents an average annual growth rate of 8.7%.

NASA has used computers extensively for both administrative systems and mission support, and these systems have functioned in a highly decentralized mode. But NASA is now making changes that will require more information sharing than at any time in its history, reports the market research and consulting firm. In selected areas, such as procurement, software management and assurance, and the Space Station program, NASA is moving away from its decentralized approach.

Historically, NASA has not always been on the cutting edge of information systems technology. But reports from oversight agencies have prompted NASA to start a wide-ranging program to intensify its automation of highly technical areas. This program includes establishing sophisticated local-area networks to facilitate information sharing, improving its own development of software, a significant upgrade of computer facilities at its centers, and implementing artificial intelligence to enhance decision-support activities.

Traditionally, NASA has used contractors more than most agencies in performing mission activities. According to Input, software products and hardware lead contracted information-systems expenditures at 24% and 23%, respectively.

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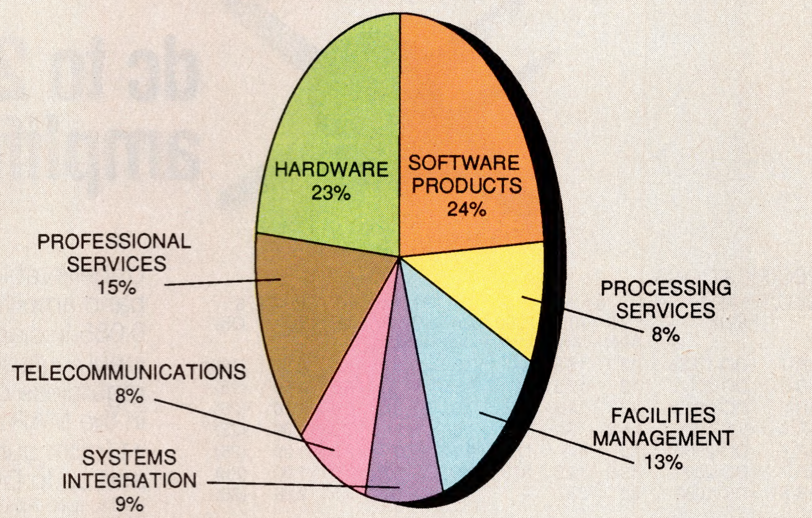


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